

DATA SHEET

TDA4855 Autosync Deflection Controller (ASDC)

Preliminary specification
File under Integrated Circuits, IC02

1996 Jul 18

Autosync Deflection Controller (ASDC)

TDA4855

FEATURES

Concept features

- Full Horizontal (H) plus Vertical (V) autosync capability
- Completely DC controllable for analog and digital concepts
- Excellent geometry control functions (e.g. automatic correction of East-West (EW) parabola during adjustment of vertical size and vertical shift)
- Flexible Switched Mode Power Supply (SMPS) function block for feedback and feed forward converters
- Horizontal focus parabola with amplitude control
- X-ray protection
- Start-up and switch-off sequence for safe operation of all power components
- Very good vertical linearity
- Internal supply voltage stabilization
- SDIP32 package.

Synchronization inputs

- Can handle all sync signals (Horizontal, Vertical, Composite and Sync-on-video)
- Combined output for video clamping, vertical blanking and protection blanking.

Horizontal section

- Extremely low jitter
- Frequency locked loop for smooth catching of line frequency
- Simple frequency preset of f_{\min} and f_{\max} by external resistors
- DC controllable wide range linear picture position
- Soft start for horizontal driver.

Vertical section

- Vertical amplitude independent of frequency
- Automatic correction of picture height for VGA350 and VGA400 modes
- DC controllable picture height, picture position and S-correction
- Differential current outputs for DC coupling to vertical booster.

EW section

- Output for DC adjustable EW parabola with smoothed top
- DC controllable picture width and trapezium correction
- Optional tracking of EW parabola with line frequency
- Prepared for additional DC controls of vertical linearity, EW-corner, EW pin balance, EW parallelogram, vertical focus by extended application.

GENERAL DESCRIPTION

The TDA4855 is a high performance and efficient solution for autosync monitors. The concept is fully DC controllable and can be used in applications with a microcontroller and stand-alone in rock bottom solutions.

The TDA4855 provides synchronization processing, H + V synchronization with full autosync capability, and very short settling times after mode changes. External power components are given a great deal of protection. The IC generates the drive waveforms for DC-coupled vertical boosters such as TDA486X and TDA8351.

The TDA4855 provides extended functions e.g. as a flexible SMPS block and an extensive set of geometry control facilities, providing excellent picture quality.

Together with the Philips TDA488X video processor family a very advanced system solution is offered.

Autosync Deflection Controller (ASDC)

TDA4855

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---------------------|--|------|-------|------|------|
| V _{CC} | supply voltage | 9.2 | – | 16 | V |
| I _{CC} | supply current | – | 49 | – | mA |
| ΔHPOS | horizontal shift adjustment range | – | ±10.5 | – | % |
| ΔVAMP | vertical size adjustment range | 60 | – | 100 | % |
| ΔVPOS | vertical shift adjustment range | – | ±11.5 | – | % |
| ΔVSCOR | vertical S-correction adjustment range | 2 | – | 46 | % |
| ΔV _{EWPAR} | EW parabola adjustment range | 0.15 | – | 3.0 | V |
| ΔV _{EWWID} | horizontal size adjustment range | 0.2 | – | 4.0 | V |
| ΔV _{EWTRP} | trapezium correction adjustment range | – | ±0.5 | – | V |
| T _{amb} | operating ambient temperature | 0 | – | 70 | °C |

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| TDA4855 | SDIP32 | plastic shrink dual in-line package; 32 leads (400 mil) | SOT232-1 |

Autosync Deflection Controller (ASDC)

TDA4855

BLOCK DIAGRAM

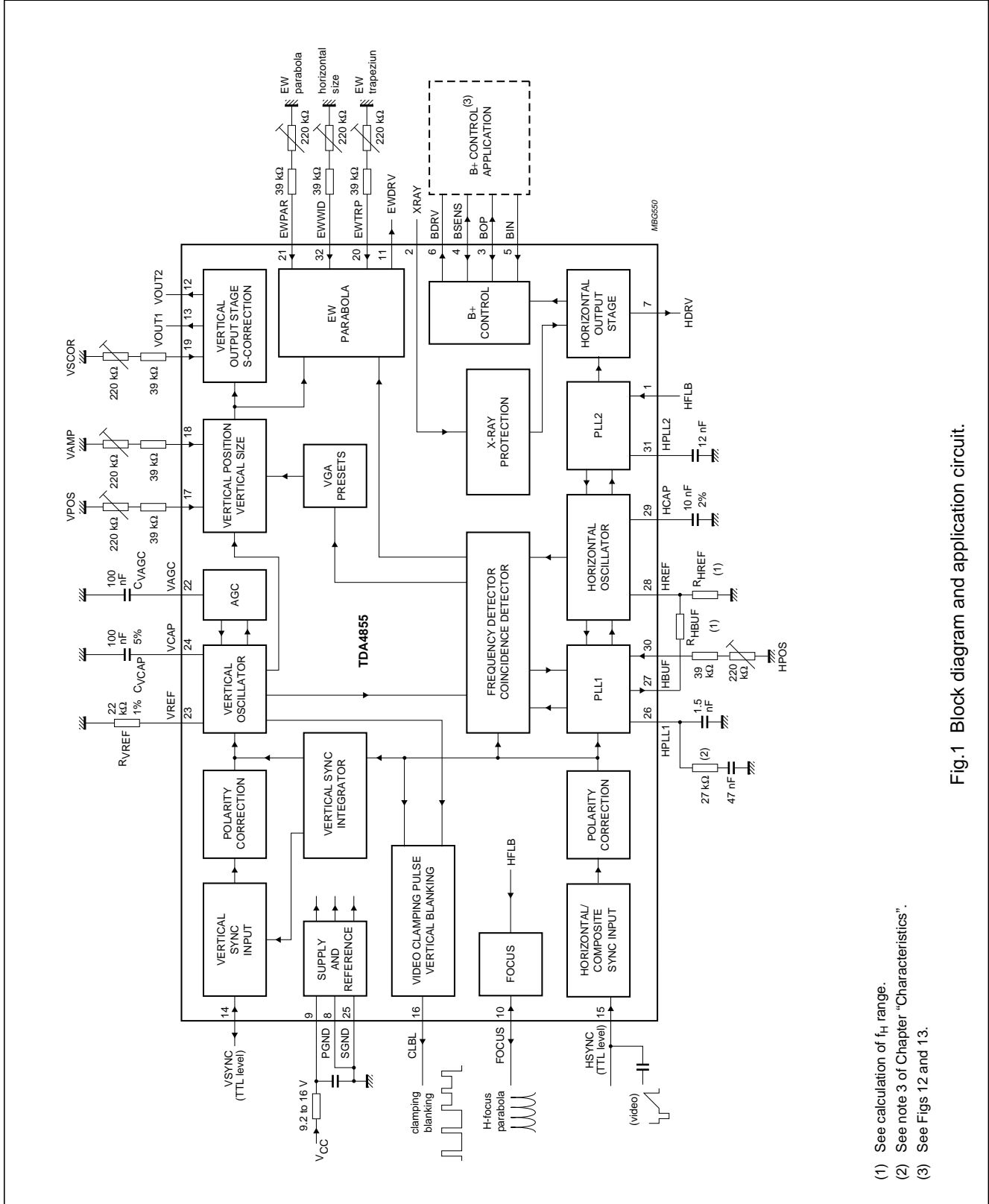


Fig.1 Block diagram and application circuit.

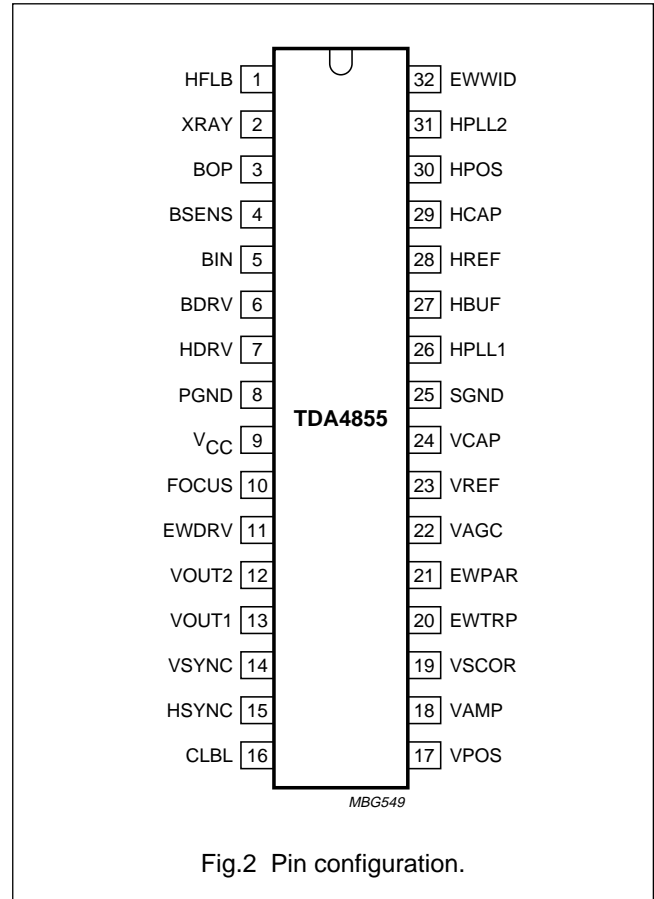
- (1) See calculation of f_H range.
- (2) See note 3 of Chapter "Characteristics".
- (3) See Figs 12 and 13.

Autosync Deflection Controller (ASDC)

TDA4855

PINNING

| SYMBOL | PIN | DESCRIPTION |
|-----------------|-----|--|
| HFLB | 1 | horizontal flyback input |
| XRAY | 2 | X-ray protection input |
| BOP | 3 | B+ control OTA output; comparator input |
| BSENS | 4 | B+ control comparator input/output |
| BIN | 5 | B+ control OTA input |
| BDRV | 6 | B+ control driver output |
| HDRV | 7 | horizontal driver output |
| PGND | 8 | power ground |
| V _{CC} | 9 | supply voltage |
| FOCUS | 10 | horizontal focus parabola input/output |
| EWDRV | 11 | EW parabola output |
| VOUT2 | 12 | vertical output 2 (ascending sawtooth) |
| VOUT1 | 13 | vertical output 1 (descending sawtooth) |
| VSYNC | 14 | vertical synchronization input/output (TTL level) |
| HSYNC | 15 | horizontal/composite synchronization input (TTL level or sync-on-video) |
| CLBL | 16 | video clamping pulse/vertical blanking and protection output |
| VPOS | 17 | vertical shift input |
| VAMP | 18 | vertical size input |
| VSCOR | 19 | vertical S-correction input |
| EWTRP | 20 | EW trapezium correction input |
| EWPAR | 21 | EW parabola amplitude input |
| VAGC | 22 | external capacitor for vertical amplitude control |
| VREF | 23 | external resistor for vertical oscillator |
| VCAP | 24 | external capacitor for vertical oscillator |
| SGND | 25 | signal ground |
| HPLL1 | 26 | external filter for PLL1 |
| HBUF | 27 | buffered f/v voltage output |
| HREF | 28 | reference current for horizontal oscillator |
| HCAP | 29 | external capacitor for horizontal oscillator |
| HPOS | 30 | horizontal shift input |
| HPLL2 | 31 | external filter for PLL2/soft start |
| EWVID | 32 | horizontal size input |



Autosync Deflection Controller (ASDC)

TDA4855

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

HSYNC (pin 15) is the input for horizontal synchronization signals, which can be DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signals. Video syncs are clamped to 1.28 V and sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to sync top.

For DC-coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4 V.

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency-locked loop.

Vertical sync integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (pin 28). The integrator output directly triggers the vertical oscillator. This signal is available at VSYNC (normally vertical sync input; pin 14), which is used as an output in this mode.

Vertical sync slicer and polarity correction

Vertical sync signals (TTL) applied to VSYNC (pin 14) are sliced at 1.4 V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity.

If a composite sync signal is detected at HSYNC, VSYNC is used as output for the integrated vertical sync (e.g. for power saving applications).

Video clamping/vertical blanking generator

The video clamping/vertical blanking signal at CLBL (pin 16) is a two-level sandcastle pulse which is especially suitable for video ICs such as the TDA488X family, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the trailing edge of the horizontal sync pulse. The width of the video clamping pulse is determined by an internal monoflop.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking.

Blanking will be activated continuously, if one of the following conditions is true:

- No horizontal flyback pulses at HFLB (pin 1)
- X-ray protection is activated
- Soft start of horizontal drive (voltage at HPLL2 (pin 31) is low)
- Supply voltage at V_{CC} (pin 9) is low (see Fig.14)
- PLL1 is unlocked while frequency-locked loop is in search mode.

Blanking will not be activated if the horizontal sync frequency is below the valid range or there are no sync pulses available.

VGA mode detector

The polarities of horizontal and vertical sync are internally detected in order to provide an automatic adjustment of vertical size for VGA350 and VGA400 modes. These automatic VGA presets are activated only if the current ratio I_{HBUF}/I_{HREF} exceeds a fixed value (see Chapter "Characteristics"). Thus it is possible to disable this function for a part of the frequency range or even completely.

Table 1 VGA modes

| MODE | HORIZONTAL/VERTICAL SYNC POLARITY | |
|--------|-----------------------------------|---|
| VGA350 | + | - |
| VGA400 | - | + |
| VGA480 | - | - |
| - | + | + |

Autosync Deflection Controller (ASDC)

TDA4855

Frequency-locked loop

The frequency-locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the

recommended maximum ratio is $\frac{f_{min}}{f_{max}} = \frac{1}{3.5}$

Larger ranges are possible by extended applications.

Without a horizontal sync signal the oscillator will be free-running at f_{min} . Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between horizontal sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. Then the internal frequency detector starts tuning the oscillator. Very small DC currents at HPLL1 (pin 26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is replaced by a normal PLL operation. This operation ensures a smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1. The frequency dependent voltage at this pin is fed internally to HBUF (pin 27) via a sample-and-hold and buffer stage. The sample-and-hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor from HBUF to HREF defines the frequency range.

See also hints for locking procedure in note 3 of Chapter "Characteristics".

PLL1 phase detector

The phase detector is a standard type using switched current sources. It compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26).

Horizontal oscillator

The horizontal oscillator is of the relaxation type and requires a capacitor of 10 nF at HCAP (pin 29). For optimum jitter performance the value of 10 nF must not be changed.

The maximum oscillator frequency is determined by a resistor from HREF to ground. A resistor from HREF to HBUF defines the frequency range.

The reference current at HREF also defines the integration time constant of the vertical sync integration.

Calculation of line frequency range

First the oscillator frequencies f_{min} and f_{max} have to be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{S(min)}$ and $f_{S(max)}$. The oscillator is driven by the difference of the currents in R_{HREF} and R_{HBUF} . At the highest oscillator frequency R_{HBUF} does not contribute to the spread. The spread will increase towards lower frequencies due to the contribution of R_{HBUF} . It is also

dependent on the ratio $n_S = \frac{f_{S(max)}}{f_{S(min)}}$

The following example is a 31.45 to 64 kHz application:

$$n_S = \frac{f_{S(max)}}{f_{S(min)}} = \frac{64 \text{ kHz}}{31.45 \text{ kHz}} = 2.04$$

Table 2 Calculation of total spread

| spread of: | for f_{max} | for f_{min} |
|----------------------|---------------|-----------------------------------|
| IC | 3% | 3% |
| C_{HCAP} | 2% | 2% |
| R_{HREF} | 1% | – |
| R_{HREF}, R_{HBUF} | – | $1\% \times (2.3 \times n_S - 1)$ |
| Total | 6% | 8.69% |

Thus the typical frequency range of the oscillator in this example is:

$$f_{max} = f_{S(max)} \times 1.06 = 67.84 \text{ kHz}$$

$$f_{min} = \frac{f_{S(min)}}{1.087} = 28.93 \text{ kHz}$$

The resistors R_{HREF} and R_{HBUF} can be calculated with the following formulae:

$$R_{HREF} = \frac{74 \times \text{kHz} \times \text{k}\Omega}{f_{max} [\text{kHz}]} = 1.091 \text{ k}\Omega$$

$$R_{HBUF} = \frac{R_{HREF} \times 1.19 \times n}{n - 1} = 2.26 \text{ k}\Omega$$

Where: $n = \frac{f_{max}}{f_{min}} = 2.35$

Autosync Deflection Controller (ASDC)

TDA4855

The spread of f_{\min} increases with the frequency

$$\text{ratio} \frac{f_{S(\max)}}{f_{S(\min)}}.$$

For higher ratios this spread can be reduced by using resistors with less tolerances.

PLL2 phase detector

The PLL2 phase detector is similar to the PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (pin 7) output pulse.

The phase between horizontal flyback and horizontal sync can be controlled at HPOS (pin 30).

If HPLL2 is pulled to ground, horizontal output pulses, vertical output currents and B+ control driver pulses are inhibited. This means, HDRV (pin 7), BDRV (pin 6) VOUT1 (pin 13) and VOUT2 (pin 12) are floating in this state. PLL2 and the frequency-locked loop are disabled, and CLBL (pin 16) provides a continuous blanking signal.

This option can be used for soft start, protection and power-down modes. When the HPLL2 voltage is released again, an automatic soft start sequence will be performed (see Fig.15).

The soft start timing is determined by the filter capacitor at HPLL2 (pin 31), which is charged with a constant current during soft start. In the beginning the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty factor is reached. At this point BDRV (pin 6), VOUT1 (pin 13) and VOUT2 (pin 12) are re-enabled. The voltage at HPLL2 continues to rise until PLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency-locked loop are enabled, and the continuous blanking at CLBL is removed.

Horizontal phase adjustment

HPOS (pin 30) provides a linear adjustment of the relative phase between the horizontal sync and oscillator sawtooth. Once adjusted, the relative phase remains constant over the whole frequency range.

Application hint: HPOS is a current input, which provides an internal reference voltage while I_{HPOS} is in the specified adjustment current range. By grounding HPOS the symmetrical control range is forced to its centre value,

therefore the phase between horizontal sync and horizontal drive pulse is only determined by PLL2.

Output stage for line drive pulses

An open collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3 V at 20 mA. To protect the line deflection transistor, the output stage is disabled (floating) for low supply voltage at V_{CC} (see Fig.14).

The duty factor of line drive pulses is slightly dependent on the actual line frequency. This ensures optimum drive conditions over the whole frequency range.

X-ray protection

The x-ray protection input XRAY (pin 2) provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold for a certain time, an internal latch switches the IC into protection mode. In this mode several pins are forced into defined states:

- Horizontal output stage (HDRV) is floating
- B+ control driver stage (BDRV) is floating
- Vertical output stages (VOUT1 and VOUT2) are floating
- CLBL provides a continuous blanking signal
- The capacitor connected to HPLL2 (pin 31) is discharged.

To reset the latch and return to normal operation, V_{CC} has to be temporarily switched off.

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of vertical amplitude after changes in sync frequency conditions. The free-running frequency $f_{\text{osc}(V)}$ is determined by the resistor R_{VREF} connected to pin 23 and the capacitor C_{VCAP} connected to pin 24. The value of R_{VREF} is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal references. Therefore the value of R_{VREF} must not be changed. Capacitor C_{VCAP} should be used to select the free-running frequency of the vertical oscillator in accordance with the following formula:

$$f_{\text{osc}(V)} = \frac{1}{10.8 \times R_{\text{VREF}} \times C_{\text{VCAP}}}$$

Autosync Deflection Controller (ASDC)

TDA4855

To achieve a stabilized amplitude the free-running frequency $f_{osc(V)}$, without adjustment, should be at least 10% lower than the minimum trigger frequency. The contributions shown in Table 3 can be assumed.

Table 3 Calculation of $f_{osc(V)}$ total spread

| Contributing elements: | |
|--|------|
| Minimum frequency offset between $f_{osc(V)}$ and lowest trigger frequency | ±10% |
| Spread of IC | ±3% |
| Spread of R_{VREF} | ±1% |
| Spread of C_{VCAP} | ±5% |
| Total | 19% |

Result for 50 to 110 Hz application:

$$f_{osc(V)} = \frac{50 \text{ Hz}}{1.19} = 42 \text{ Hz}$$

Application hint: VAGC (pin 22) has a high input impedance during scan, thus the pin must not be loaded externally. Otherwise non-linearities in the vertical output currents may occur due to the changing charge current during scan.

Application hint: The full vertical sync range of 1 : 2.5 can be made usable by incorporating an adjustment of the free-running frequency. Also the complete sync range can be shifted to higher frequencies (e.g. 70 to 160 Hz) by reducing the value of C_{VCAP} .

Adjustment of vertical size, vertical shift and S-correction

VPOS (pin 17) is the input for the DC adjustable vertical picture shift. This pin provides a phase shift at the sawtooth output VOUT1 and VOUT2 (pins 13 and 12) and the EW drive output EWDRV (pin 11) in such a way, that the whole picture moves vertically while maintaining the correct geometry.

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via input VAMP (pin 18). This can be a combination of a DC adjustment and a dynamic waveform modulation.

VSCOR (pin 19) is used to adjust the amount of vertical S-correction in the output signal.

The adjustments for vertical size and vertical shift also affect the waveforms of the EW parabola and the vertical S-correction. The result of this interaction is that no

readjustment of these parameters is necessary after an adjustment of vertical picture size or position.

Application hint: VPOS is a current input, which provides an internal reference voltage while I_{VPOS} is in the specified adjustment current range. By grounding VPOS (pin 17) the symmetrical control range is forced to its centre value.

Application hint: VSCOR is a current input at 5 V. Superimposed on this level is a very small positive-going vertical sawtooth, intended to modulate an external long-tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as vertical tilt or vertical linearity (see Fig.17).

EW parabola (including horizontal size and trapezium correction)

EWDRV (pin 11) provides a complete EW drive waveform. EW parabola amplitude, DC shift (horizontal size) and trapezium correction can be controlled via separate DC inputs.

EWPARG (pin 21) is used to adjust the parabola amplitude. This can be a combination of a DC adjustment and a dynamic waveform modulation.

The EW parabola amplitude also tracks with vertical picture size. The parabola waveform itself tracks with the adjustment for vertical picture shift (VPOS). Additional effort has been taken to generate a smooth waveform at the top of the parabola. This is to avoid ringing in the horizontal output stage.

EWWDID (pin 32) offers two modes of operation:

1. Mode 1
Horizontal size is DC controlled via EWWDID (pin 32) and causes a DC shift at the EWDRV output. Also the complete waveform is multiplied internally by a signal proportional to the line frequency (which is detected via the current at HREF (pin 28)). This mode is to be used for driving EW modulator stages which require a voltage proportional to the line frequency.
2. Mode 2
EWWDID (pin 32) is grounded. Then EWDRV is no longer multiplied by the line frequency. The DC adjustment for horizontal size must be added to the input of the B+ control amplifier BIN (pin 5). This mode is to be used for driving EW modulators which require a voltage independent of the line frequency.

EWTRP (pin 20) is used to adjust the amount of trapezium correction in the EW drive waveform.

Autosync Deflection Controller (ASDC)

TDA4855

Application hint: EWTRP (pin 20) is a current input at 5 V. Superimposed on this level is a very small vertical parabola with positive tips, intended to modulate an external long-tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as EW-corner, vertical focus or EW pin balance (see Fig.17).

Application hint: By grounding EWTRP (pin 20) the symmetrical control range is forced to its centre value.

Dynamic focus section

This section generates a horizontal parabola waveform for dynamic focus applications. The amplitude of this parabola is internally stabilized, thus it is independent from the line frequency.

FOCUS (pin 10) is designed as a current sink. The peak-to-peak amplitude of the output current can be adjusted by forcing the voltage at pin 10 to a value between 1 and 4 V.

B+ control function block

The B+ control function block of the ASDC consists of an Operational Transconductance Amplifier (OTA), a voltage comparator, a flip-flop and a discharge circuit. This configuration allows easy applications for different B+ control concepts.

GENERAL DESCRIPTION

The non-inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (pin 5). An internal clamping circuit limits the maximum positive output voltage of the OTA.

The output itself is connected to BOP (pin 3) and to the inverting input of the voltage comparator.

The non-inverting input of the voltage comparator can be accessed via BSENS (pin 4).

B+ drive pulses are generated by an internal flip-flop and fed to BDRV (pin 6) via an open collector output stage. This flip-flop will be set at the rising edge of the signal at HDRV (pin 7). The falling edge of the output signal at BDRV has a defined delay of $t_{d(BDRV)}$ to the rising edge of the HDRV pulse. When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip-flop, and therefore the open collector stage at BDRV is floating again.

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a low level output voltage (see Figs 12 and 13), thus it requires an external inverting driver stage.

The B+ function block can be used for B+ deflection modulators in either of two modes:

- Feedback mode (see Fig.12)

In this application the OTA is used as an error amplifier with a limited output voltage range. The flip-flop will be set at the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS taken from the current sense resistor exceeds the voltage at BOP.

If no reset is generated within a line period, the rising edge of the next HDRV pulse forces the flip-flop to reset. The flip-flop is set immediately after the voltage at BSENS has dropped below the threshold voltage $V_{RESTART(BSENS)}$.

- Feed forward mode (see Fig.13)

This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip-flop is reset by the internal voltage comparator. Now the capacitor will be discharged with a constant current until the internally controlled stop level $V_{STOP(BSENS)}$ is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip-flop again and disables the discharge circuit.

If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip-flop (Fig.13). When the voltage at BSENS reaches the threshold voltage $V_{RESTART(BSENS)}$, the discharge circuit will be disabled automatically and the flip-flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the B+ control drive pulse by the relationship of charge current to discharge current.

Autosync Deflection Controller (ASDC)

TDA4855

Supply voltage stabilizer, references and protection

The ASDC provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference especially designed for low-noise is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

A special protection mode has been implemented in order to protect the deflection stages and the picture tube during start-up, shut-down and fault conditions. This protection mode can be activated as shown in Table 4.

Table 4 Activation of protection mode

| ACTIVATION | RESET |
|---|-------------------------|
| Low supply voltage at pin 9 | increase supply voltage |
| X-ray protection XRAY (pin 2) triggered | remove supply voltage |
| HPLL2 (pin 31) pulled to ground | release pin 31 |

When protection mode is active, several pins of the ASDC are forced into a defined state:

- HDRV (horizontal driver output) is floating
- BDRV (B+ control driver output) is floating
- VOUT1 and VOUT2 (vertical outputs) are floating
- CLBL provides a continuous blanking signal
- The capacitor at HPLL2 is discharged.

If the protection mode is activated via the supply voltage at pin 9, all these actions will be performed in a well defined sequence (see Fig.14). For activation via X-ray protection or HPLL2 all actions will occur simultaneously.

The return to normal operation is performed in accordance with the start-up sequence in Fig.14a, if the reset was caused by the supply voltage at pin 9. The first action with increasing supply voltage is the activation of continuous blanking at CLBL. When the threshold for activation of HDRV is passed, an internal current begins to charge the external capacitor at HPLL2 and a PLL2 soft start sequence is performed (see Fig.15). In the beginning of this phase the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. Then the PLL2 voltage passes the threshold for activation of BDRV, VOUT1 and VOUT2.

For activation of these pins not only the PLL2 voltage, but also the supply voltage must have passed the appropriate threshold. A last pair of thresholds has to be passed by PLL2 voltage **and** supply voltage before the continuous blanking is finally removed, and the operation of PLL2 and frequency-locked loop is enabled.

A return to the normal operation by releasing the voltage at HPLL2 will lead to a slightly different sequence. Here the activation of all functions is influenced only by the voltage at HPLL2 (see Fig.15).

Application hint: Internal discharge of the capacitor at HPLL2 will only be performed, if the protection mode was activated via the supply voltage or X-ray protection.

Autosync Deflection Controller (ASDC)

TDA4855

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages measured with respect to ground.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---------------------|---|-------|-------|------|
| V _{CC} | supply voltage | -0.5 | +16 | V |
| V _{I(n)} | input voltages | | | |
| | BIN | -0.5 | +6.0 | V |
| | HSYNC, VPOS, VAMP, VSCOR, VREF, HREF and HPOS | -0.5 | +6.5 | V |
| | XRAY | -0.5 | +8.0 | V |
| V _{O(n)} | output voltages | | | |
| | VOUT1 and VOUT2 | -0.5 | +6.5 | V |
| | BDRV and HDRV | -0.5 | +16 | V |
| V _{I/O(n)} | input/output voltages | | | |
| | BOP and BSENS | -0.5 | +6.0 | V |
| | FOCUS and VSYNC | -0.5 | +6.5 | V |
| I _{HDRV} | horizontal driver output current | - | 100 | mA |
| I _{HFLB} | horizontal flyback input current | -10 | +10 | mA |
| I _{CLBL} | video clamping pulse/vertical blanking output current | - | -10 | mA |
| I _{BOP} | B+ control OTA output current | - | 1 | mA |
| I _{BDRV} | B+ control driver output current | - | 50 | mA |
| I _{EWDRV} | EW driver output current | - | -5 | mA |
| T _{amb} | operating ambient temperature | 0 | 70 | °C |
| T _j | junction temperature | - | 150 | °C |
| T _{stg} | storage temperature | -55 | +150 | °C |
| V _{esd} | electrostatic discharge for all pins (note 1) | | | |
| | machine model | -400 | +400 | V |
| | human body model | -3000 | +3000 | V |

Note

1. Machine model: 200 pF, 25 Ω, 2.5 μH; human body model: 100 pF, 1500 Ω, 7.5 μH.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------------|---|-------|------|
| R _{th j-a} | thermal resistance from junction to ambient in free air | 55 | K/W |

QUALITY SPECIFICATION

In accordance with "URF-4-2-59/601", EMC emission/immunity test in accordance with "DIS 1000 4.6" (IEC 801.6)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|---------------|------------|------|------|------|------|
| V _{EMC} | emission test | note 1 | - | 1.5 | - | mV |
| | immunity test | note 1 | - | 2.0 | - | V |

Note

1. Tests are performed with application reference board. Tests with other boards will have different results.

Autosync Deflection Controller (ASDC)

TDA4855

CHARACTERISTICS $V_{CC} = 12\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; peripheral components in accordance with Fig.1; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--|------|------|----------|---------------|
| Horizontal sync separator | | | | | | |
| INPUT CHARACTERISTICS FOR DC-COUPLED TTL SIGNALS [HSYNC (PIN 15)] | | | | | | |
| $V_{DC(HSYNC)}$ | sync input signal voltage | | 1.7 | – | – | V |
| | slicing voltage level | | 1.2 | 1.4 | 1.6 | V |
| $t_{r(HSYNC)}$ | rise time of sync pulse | | 10 | – | 500 | ns |
| $t_{f(HSYNC)}$ | fall time of sync pulse | | 10 | – | 500 | ns |
| $t_{W(HSYNC)}$ | minimum width of sync pulse | | 0.7 | – | – | μs |
| $I_{DC(HSYNC)}$ | input current | $V_{HSYNC} = 0.8\text{ V}$ | – | – | –200 | μA |
| | | $V_{HSYNC} = 5.5\text{ V}$ | – | – | 10 | μA |
| INPUT CHARACTERISTICS FOR AC-COUPLED VIDEO SIGNALS (SYNC-ON-VIDEO, NEGATIVE SYNC POLARITY) | | | | | | |
| $V_{AC(HSYNC)}$ | sync amplitude of video input signal voltage | | – | 300 | – | mV |
| | slicing voltage level (measured from top sync) | source resistance $R_S = 50\ \Omega$ | 90 | 120 | 150 | mV |
| $V_{clamp(HSYNC)}$ | top sync clamping voltage level | | 1.1 | 1.28 | 1.5 | V |
| $I_C(HSYNC)$ | charge current for coupling capacitor | $V_{HSYNC} > V_{clamp(HSYNC)}$ | 1.7 | 2.4 | 3.4 | μA |
| $t_{HSYNC(min)}$ | minimum width of sync pulse | | 0.7 | – | – | μs |
| $R_{S(max)}$ | maximum source resistance | duty factor = 7% | – | – | 1500 | Ω |
| $r_{diff(HSYNC)}$ | differential input resistance | during sync | – | 80 | – | Ω |
| Automatic polarity correction for horizontal sync | | | | | | |
| $\frac{t_{P(H)}}{t_H}$ | horizontal sync pulse width related to t_H | $f_H < 45\text{ kHz}$ | – | – | 20 | % |
| | | $f_H > 45\text{ kHz}$ | – | – | 25 | % |
| $t_{P(H)}$ | delay time for changing polarity | | 0.3 | – | 1.8 | ms |
| Vertical sync integrator | | | | | | |
| $t_{int(V)}$ | integration time for generation of a vertical trigger pulse | $f_H = 31.45\text{ kHz}$; $I_{HREF} = 1.052\text{ mA}$ | 7 | 10 | 13 | μs |
| | | $f_H = 64\text{ kHz}$; $I_{HREF} = 2.141\text{ mA}$ | 3.9 | 5.7 | 6.5 | μs |
| | | $f_H = 100\text{ kHz}$; $I_{HREF} = 3.345\text{ mA}$ | 2.5 | 3.8 | 4.5 | μs |
| Vertical sync slicer (DC-coupled, TTL compatible) [VSYNC (pin 14)] | | | | | | |
| V_{VSYNC} | sync input signal voltage | | 1.7 | – | – | V |
| | slicing voltage level | | 1.2 | 1.4 | 1.6 | V |
| I_{VSYNC} | input current | $0\text{ V} < V_{VSYNC} < 5.5\text{ V}$ | – | – | ± 10 | μA |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|--|------|------|-------|---------|
| VERTICAL SYNC OUTPUT AT VSYNC (PIN 14) DURING COMPOSITE SYNC AT HSYNC (PIN 15) | | | | | | |
| I_{VSYNC} | output current | during internal vertical sync | -0.7 | -1.0 | -1.35 | mA |
| V_{VSYNC} | internal clamping voltage level | during internal vertical sync | 4.4 | 4.8 | 5.2 | V |
| | steepness of slopes | | - | 300 | - | ns/mA |
| Automatic polarity correction for vertical sync | | | | | | |
| $t_{VSYNC(max)}$ | maximum width of vertical sync pulse | | - | - | 300 | μ s |
| $t_{d(VPOL)}$ | delay for changing polarity | | 0.3 | - | 1.8 | ms |
| Video clamping/vertical blanking output [CLBL (pin 16)] | | | | | | |
| $t_{clamp(CLBL)}$ | width of video clamping pulse | measured at $V_{CLBL} = 3$ V | 0.6 | 0.7 | 0.8 | μ s |
| $V_{clamp(CLBL)}$ | top voltage level of video clamping pulse | | 4.32 | 4.75 | 5.23 | V |
| $t_{d(clamp)}$ | delay between trailing edge of horizontal sync and start of video clamping pulse | clamping pulse triggered on trailing edge of horizontal sync | - | 130 | - | ns |
| $t_{clamp(max)}$ | maximum duration of video clamping pulse referenced to end of horizontal sync | measured at $V_{CLBL} = 3$ V | - | - | 1.0 | μ s |
| TC_{clamp} | temperature coefficient of $V_{clamp(CLBL)}$ | | - | +4 | - | mV/K |
| | steepness of slopes for clamping pulse | $R_L = 1$ M Ω ; $C_L = 20$ pF | - | 50 | - | ns/V |
| $V_{blank(CLBL)}$ | top voltage level of vertical blanking pulse | notes 1 and 2 | 1.7 | 1.9 | 2.1 | V |
| $t_{blank(CLBL)}$ | width of vertical blanking pulse | VGA presets active | 500 | 575 | 650 | μ s |
| | | VGA presets disabled | 240 | 300 | 360 | μ s |
| TC_{blank} | temperature coefficient of $V_{blank(CLBL)}$ | | - | +2 | - | mV/K |
| $V_{scan(CLBL)}$ | output voltage during vertical scan | $I_{CLBL} = 0$ | 0.59 | 0.63 | 0.67 | V |
| TC_{scan} | temperature coefficient of $V_{scan(CLBL)}$ | | - | -2 | - | mV/K |
| $I_{sink(CLBL)}$ | internal sink current | | 2.4 | - | - | mA |
| $I_{load(CLBL)}$ | external load current | | - | - | -3.0 | mA |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|-------|-------|-----------|--------------------|
| PLL1 phase comparator and frequency-locked loop [HPLL1 (pin 26) and HBUF (pin 27)] | | | | | | |
| $t_{\text{HSYNC(max)}}$ | maximum width of horizontal sync pulse (referenced to line period) | $f_{\text{H}} < 45 \text{ kHz}$; note 3 | – | – | 20 | % |
| | | $f_{\text{H}} > 45 \text{ kHz}$; note 3 | – | – | 25 | % |
| $t_{\text{lock(HPLL1)}}$ | total lock-in time of PLL1 | | – | 40 | 80 | ms |
| V_{HPLL1} | control voltage | notes 4 and 5 | | | | |
| V_{HBUF} | buffered f/v voltage at HBUF (pin 27) | $f_{\text{H(min)}}$; note 6 | – | 5.6 | – | V |
| | | $f_{\text{H(max)}}$; note 6 | – | 2.5 | – | V |
| $I_{\text{load(HBUF)}}$ | maximum load current | | – | – | –4.0 | mA |
| ADJUSTMENT OF HORIZONTAL PICTURE POSITION | | | | | | |
| ΔHPOS | horizontal shift adjustment range (referenced to horizontal period) | $I_{\text{HSHIFT}} = 0$ | – | –10.5 | – | % |
| | | $I_{\text{HSHIFT}} = -135 \mu\text{A}$ | – | +10.5 | – | % |
| I_{HPOS} | input current | $\Delta\text{HPOS} = +10.5\%$ | –110 | –120 | –135 | μA |
| | | $\Delta\text{HPOS} = -10.5\%$ | – | 0 | – | μA |
| $V_{\text{ref(HPOS)}}$ | reference voltage at input | note 7 | – | 5.1 | – | V |
| $V_{\text{off(HPOS)}}$ | picture shift is centred if HPOS (pin 30) is forced to ground | | 0 | – | 0.1 | V |
| Horizontal oscillator [HCAP (pin 29) and HREF (pin 28)] | | | | | | |
| $f_{\text{H(0)}}$ | free-running frequency without PLL1 action (for testing only) | $R_{\text{HBUF}} = \infty$; $R_{\text{HREF}} = 2.4 \text{ k}\Omega$; $C_{\text{HCAP}} = 10 \text{ nF}$; note 5 | 30.53 | 31.45 | 32.39 | kHz |
| $\Delta f_{\text{H(0)}}$ | spread of free-running frequency (excluding spread of external components) | | – | – | ± 3.0 | % |
| TC | temperature coefficient of free-running frequency | | –100 | 0 | +100 | $10^{-6}/\text{K}$ |
| $f_{\text{H(max)}}$ | maximum oscillator frequency | | – | – | 130 | kHz |
| V_{HREF} | voltage at input for reference current | | 2.43 | 2.55 | 2.68 | V |
| PLL2 phase detector [HFLB (pin 1) and HPLL2 (pin 31)] | | | | | | |
| $\Delta\phi_{\text{PLL2}}$ | PLL2 control (advance of horizontal drive with respect to middle of horizontal flyback) | maximum advance | 36 | – | – | % |
| | | minimum advance | – | 7 | – | % |
| $t_{\text{d(HFLB)}}$ | delay between middle of horizontal sync and middle of horizontal flyback | HPOS (pin 30) grounded | – | 200 | – | ns |
| $V_{\text{PROT(HPLL2)}}$ | maximum voltage for PLL2 protection mode/soft start | | – | 4.4 | – | V |
| $I_{\text{charge(HPLL2)}}$ | charge current for external capacitor during soft start | $V_{\text{HPLL2}} < 3.7 \text{ V}$ | – | 15 | – | μA |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|-------|------|------|
| HORIZONTAL FLYBACK INPUT [HFLB (PIN 1)] | | | | | | |
| V _{HFLB} | positive clamping level | I _{HFLB} = 5 mA | – | 5.5 | – | V |
| | negative clamping level | I _{HFLB} = –1 mA | – | –0.75 | – | V |
| I _{HFLB} | positive clamping current | | – | – | 6 | mA |
| | negative clamping current | | – | – | –2 | mA |
| V _{HFLB} | slicing level | | – | 2.8 | – | V |
| Output stage for line driver pulses [HDRV (pin 7)] | | | | | | |
| OPEN COLLECTOR OUTPUT STAGE | | | | | | |
| V _{HDRV} | saturation voltage | I _{HDRV} = 20 mA | – | – | 0.3 | V |
| | | I _{HDRV} = 60 mA | – | – | 0.8 | V |
| I _{leakage(HDRV)} | output leakage current | V _{HDRV} = 16 V | – | – | 10 | μA |
| AUTOMATIC VARIATION OF DUTY FACTOR | | | | | | |
| t _{HDRV(OFF)} /t _H | relative t _{OFF} time of HDRV output; measured at V _{HDRV} = 3 V; HDRV duty factor is determined by the relation I _{HREF} /I _{VREF} | I _{HDRV} = 20 mA; f _H = 31.45 kHz; see Fig.9 | 42 | 45 | 48 | % |
| | | I _{HDRV} = 20 mA; f _H = 57 kHz; see Fig.9 | 45 | 46.3 | 47.7 | % |
| | | I _{HDRV} = 20 mA; f _H = 90 kHz; see Fig.9 | 46.6 | 48 | 49.4 | % |
| X-ray protection [XRAY (pin 2)] | | | | | | |
| V _{XRAY} | slicing voltage level | | 6.14 | 6.38 | 6.64 | V |
| t _{W(XRAY)} | minimum width of trigger pulse | | 10 | – | – | μs |
| R _{I(XRAY)} | input resistance at XRAY (pin 2) | V _{XRAY} < 6.38 V + V _{BE} | 500 | – | – | kΩ |
| | | V _{XRAY} > 6.38 V + V _{BE} | – | 5 | – | kΩ |
| V _{RESET(VCC)} | supply voltage for reset of X-ray latch | | – | 5.6 | – | V |
| Vertical oscillator (oscillator frequency in application without adjustment of free-running frequency f_{v(o)}) | | | | | | |
| f _v | free-running frequency | R _{VREF} = 22 kΩ; C _{VCAP} = 100 nF | 40 | 42 | 43.3 | Hz |
| f _{v(o)} | vertical frequency catching range | constant amplitude; notes 8, 9 and 10 | 50 | – | 110 | Hz |
| V _{VREF} | voltage at reference input for vertical oscillator | | – | 3.0 | – | V |
| t _{d(scan)} | delay between trigger pulse and start of ramp at VCAP (pin 24) (width of vertical blanking pulse) | VGA presets active | 500 | 575 | 650 | μs |
| | | VGA presets disabled | 240 | 300 | 360 | μs |
| I _{VAGC} | control currents of amplitude control | | ±120 | ±200 | ±300 | μA |
| C _{VAGC} | external capacitor at VAGC (pin 22) | | – | – | 150 | nF |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|------------------------------------|------|-------|-----------|---------|
| Differential vertical current outputs | | | | | | |
| ADJUSTMENT OF VERTICAL SIZE (see Figs 3 to 8) [VAMP (PIN 18)] | | | | | | |
| $\Delta VAMP$ | vertical size adjustment range (referenced to nominal vertical size) | $I_{VAMP} = 0$; note 11 | – | 60 | – | % |
| | | $I_{VAMP} = -135 \mu A$; note 11 | – | 100 | – | % |
| I_{VAMP} | input current for maximum amplitude (100%) | | –110 | –120 | –135 | μA |
| | input current for minimum amplitude (60%) | | – | 0 | – | μA |
| $V_{ref(VAMP)}$ | reference voltage at input | | – | 5.0 | – | V |
| PRESETS FOR VGA MODE DEPENDENT VERTICAL SIZE | | | | | | |
| I_{HBUF}/I_{HREF} | minimum current ratio I_{HBUF}/I_{HREF} for enable of VGA presets | note 12 | 2.25 | 2.5 | 2.75 | |
| $\Delta VAMP$ | variation of vertical size for detected VGA modes (reference for all amplitude settings is VGA480 mode) | VGA350 | – | 116.8 | – | % |
| | | VGA400 | – | 102.2 | – | % |
| | | VGA480 | – | 100.0 | – | % |
| ADJUSTMENT OF VERTICAL SHIFT (see Figs 3 to 8) [VPOS (PIN 17)] | | | | | | |
| $\Delta VPOS$ | vertical shift adjustment range (referenced to 100% vertical size) | $I_{VPOS} = -135 \mu A$; note 11 | – | –11.5 | – | % |
| | | $I_{VPOS} = 0$; note 11 | – | +11.5 | – | % |
| I_{VPOS} | input current for maximum shift-up | | –110 | –120 | –135 | μA |
| | input current for maximum shift-down | | – | 0 | – | μA |
| $V_{ref(VPOS)}$ | reference voltage at input | | – | 5.0 | – | V |
| $V_{off(VPOS)}$ | vertical shift is centred if VPOS (pin 17) is forced to ground | | 0 | – | 0.1 | V |
| ADJUSTMENT OF VERTICAL S-CORRECTION (see Figs 3 to 8) [VSCOR (PIN 19)] | | | | | | |
| $\Delta VSCOR$ | vertical S-correction adjustment range | $I_{VSCOR} = 0$; note 11 | – | 2 | – | % |
| | | $I_{VSCOR} = -135 \mu A$; note 11 | – | 46 | – | % |
| I_{VSCOR} | input current for maximum S-correction | | –110 | –120 | –135 | μA |
| | input current for minimum S-correction | | – | 0 | – | μA |
| $\delta VSCOR$ | symmetry error of S-correction | maximum $\Delta VSCOR$ | – | – | ± 0.7 | % |
| $V_{ref(VSCOR)}$ | reference voltage at input | | – | 5.0 | – | V |
| $V_{SAWM(p-p)}$ | voltage amplitude of superimposed logarithmic sawtooth (peak-to-peak value) | note 13 | – | – | 145 | mV |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--|------|------|-----------|-------------|
| Vertical output stage [VOUT1 (pin 13) and VOUT2 (pin 12)] | | | | | | |
| $\Delta I_{VOUT(nom)}$ | nominal differential output current (peak-to-peak value) ($ \Delta I_{VOUT} = I_{VOUT1} - I_{VOUT2}$) | nominal settings; note 11 | 0.76 | 0.85 | 0.94 | mA |
| $\Delta I_{VOUT(max)}$ | maximum differential output current (peak value) ($ \Delta I_{VOUT} = I_{VOUT1} - I_{VOUT2}$) | | 0.54 | 0.6 | 0.66 | mA |
| V_{VOUT1}, V_{VOUT2} | allowed voltage at outputs | | 0 | – | 4.2 | V |
| $\delta V_{(offset)}$ | maximum offset error of vertical output currents | nominal settings; note 11 | – | – | ± 2.5 | % |
| $\delta V_{(lin)}$ | maximum linearity error of vertical output currents | nominal settings; note 11 | – | – | ± 1.5 | % |
| EW drive output | | | | | | |
| EW DRIVE OUTPUT STAGE [EWDRV (PIN 11)] | | | | | | |
| V_{EWDRV} | bottom output voltage (internally stabilized) | $V_{PAR(EWDRV)} = 0$; $V_{DC(EWDRV)} = 0$; EWTRP centred | 1.05 | 1.2 | 1.35 | V |
| | maximum output voltage | note 14 | 7.0 | – | – | V |
| I_{EWDRV} | output load current | | – | – | ± 2.0 | mA |
| TC_{EWDRV} | temperature coefficient of output signal | | – | – | 600 | $10^{-6}/K$ |
| ADJUSTMENT OF EW PARABOLA AMPLITUDE (see Figs 3 to 8) [EWPAR (PIN 21)] | | | | | | |
| $V_{PAR(EWDRV)}$ | parabola amplitude | $I_{EWPAR} = 0$; note 11 | – | 0.05 | – | V |
| | | $I_{EWPAR} = -135 \mu A$; note 11 | – | 3 | – | V |
| I_{EWPAR} | input current for maximum amplitude | | –110 | –120 | –135 | μA |
| | input current for minimum amplitude | | – | 0 | – | μA |
| $V_{ref(EWPAR)}$ | reference voltage at input | | – | 5.0 | – | V |
| ADJUSTMENT OF HORIZONTAL SIZE (see Figs 3 to 8) [EWWID (PIN 32)] | | | | | | |
| $V_{DC(EWDRV)}$ | EW parabola DC voltage shift | $I_{EWWID} = -135 \mu A$; note 11 | – | 0.1 | – | V |
| | | $I_{EWWID} = 0$; note 11 | – | 4.2 | – | V |
| I_{EWWID} | input current for maximum DC shift | | – | 0 | – | μA |
| | input current for minimum DC shift | | –110 | –120 | –135 | μA |
| $V_{ref(EWWID)}$ | reference voltage at input | | – | 5.0 | – | V |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|------|------|------|---------------|
| ADJUSTMENT OF TRAPEZIUM CORRECTION (see Figs 3 to 8) [EWTRP (PIN 20)] | | | | | | |
| $V_{TRP(EWDRV)}$ | trapezium correction voltage | $I_{EWTRP} = 0$; note 11 | – | –0.5 | – | V |
| | | $I_{EWTRP} = -135 \mu\text{A}$; note 11 | – | +0.5 | – | V |
| I_{EWTRP} | input current for maximum positive trapezium correction | | –110 | –120 | –135 | μA |
| | input current for maximum negative trapezium correction | | – | 0 | – | μA |
| $V_{ref(EWTRP)}$ | reference voltage at input | | – | 5.0 | – | V |
| $V_{off(EWTRP)}$ | trapezium correction is centred if EWTRP (pin 20) is forced to ground | | 0 | – | 0.1 | V |
| $V_{PARM(p-p)}$ | amplitude of superimposed logarithmic parabola (peak-to-peak value) | note 15 | – | – | 145 | mV |
| TRACKING OF EWDRV OUTPUT SIGNAL WITH f_H PROPORTIONAL VOLTAGE | | | | | | |
| $f_{H(MULTI)}$ | f_H range for tracking | | 24 | – | 80 | kHz |
| $V_{PAR(EWDRV)}$ | parabola amplitude at EWDRV (pin 11) | $I_{HREF} = 1.052 \text{ mA}$; $f_H = 31.45 \text{ kHz}$; note 16 | 1.3 | 1.45 | 1.6 | V |
| | | $I_{HREF} = 2.341 \text{ mA}$; $f_H = 70 \text{ kHz}$; note 16 | 2.7 | 3.0 | 3.3 | V |
| | | function disabled; note 16 | 2.7 | 3.0 | 3.3 | V |
| δV_{EWDRV} | linearity error of f_H tracking | | – | – | 8 | % |
| V_{EWWID} | voltage range to inhibit tracking | | 0 | – | 0.1 | V |
| Focus section [FOCUS (pin 10)] | | | | | | |
| $I_{FOCUS(p-p)}$ | amplitude of horizontal parabola (peak-to-peak value) | $V_{FOCUS} = 1 \text{ V}$ | – | 0.03 | – | mA |
| | | $V_{FOCUS} = 4 \text{ V}$ | – | 1 | – | mA |
| $V_{FOCUS(min)}$ | input voltage for minimum horizontal parabola amplitude | | 0.9 | 1.0 | 1.1 | V |
| $V_{FOCUS(max)}$ | input voltage for maximum horizontal parabola amplitude | | 3.65 | 4.0 | 4.4 | V |

Autosync Deflection Controller (ASDC)

TDA4855

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--|------|-----------|---------|---------|
| B+ control section (see Figs 12 and 13) | | | | | | |
| TRANSCONDUCTANCE AMPLIFIER [BIN (PIN 5) AND BOP (PIN 3)] | | | | | | |
| V_{BIN} | input voltage | | 0 | – | 5.25 | V |
| $I_{BIN(max)}$ | maximum input current | | – | – | ± 1 | μA |
| $V_{ref(int)}$ | reference voltage at internal non-inverting input of OTA | | 2.37 | 2.5 | 2.58 | V |
| $V_{BOP(min)}$ | minimum output voltage | | – | 0.4 | – | V |
| $V_{BOP(max)}$ | maximum output voltage | $I_{BOP} < 1 \text{ mA}$ | 5 | 5.3 | 5.6 | V |
| $I_{BOP(max)}$ | maximum output current | | – | ± 500 | – | μA |
| g | transconductance of OTA | note 17 | 30 | 50 | 70 | mS |
| G_{open} | open-loop gain | note 18 | – | 86 | – | dB |
| C_{BOP} | minimum value of capacitor at BOP (pin 3) | | 4.7 | – | – | nF |
| VOLTAGE COMPARATOR [BSENS (PIN 4)] | | | | | | |
| V_{BSENS} | voltage range of positive comparator input | | 0 | – | 5 | V |
| V_{BOP} | voltage range of negative comparator input | | 0 | – | 5 | V |
| I_{BSENS} | maximum leakage current | discharge disabled | – | – | –2 | μA |
| OPEN COLLECTOR OUTPUT STAGE [BDRV (PIN 6)] | | | | | | |
| $I_{BDRV(max)}$ | maximum output current | | 20 | – | – | mA |
| $I_{leakage(BDRV)}$ | output leakage current | $V_{BDRV} = 16 \text{ V}$ | – | – | 3 | μA |
| $V_{sat(BDRV)}$ | saturation voltage | $I_{BDRV} < 20 \text{ mA}$ | – | – | 300 | mV |
| $t_{off(min)}$ | minimum off-time | | – | 250 | – | ns |
| $t_d(BDRV)$ | delay between BDRV pulse and HDRV pulse | measured at $V_{HDRV}, V_{BDRV} = 3 \text{ V}$ | – | 500 | – | ns |
| BSENS DISCHARGE CIRCUIT | | | | | | |
| $V_{STOP(BSENS)}$ | discharge stop level | capacitive load; $I_{BSENS} = 0.5 \text{ mA}$ | 0.85 | 1.0 | 1.15 | V |
| $I_{DISC(BSENS)}$ | discharge current | $V_{BSENS} > 2.5 \text{ V}$ | 4.5 | 6 | 7.5 | mA |
| $V_{RESTART(BSENS)}$ | threshold voltage for restart | fault condition | 1.2 | 1.3 | 1.4 | V |
| C_{BSENS} | minimum value of capacitor at BSENS (pin 4) | | 2 | – | – | nF |
| Internal reference, supply voltage and protection | | | | | | |
| $V_{STAB(VCC)}$ | external supply voltage for complete stabilization of all internal references | | 9.2 | – | 16 | V |
| I_{VCC} | supply current | | – | 49 | – | mA |
| PSRR | power supply rejection ratio of internal supply voltage | $f = 1 \text{ kHz}$ | 50 | – | – | dB |

Autosync Deflection Controller (ASDC)

TDA4855

Notes to the characteristics

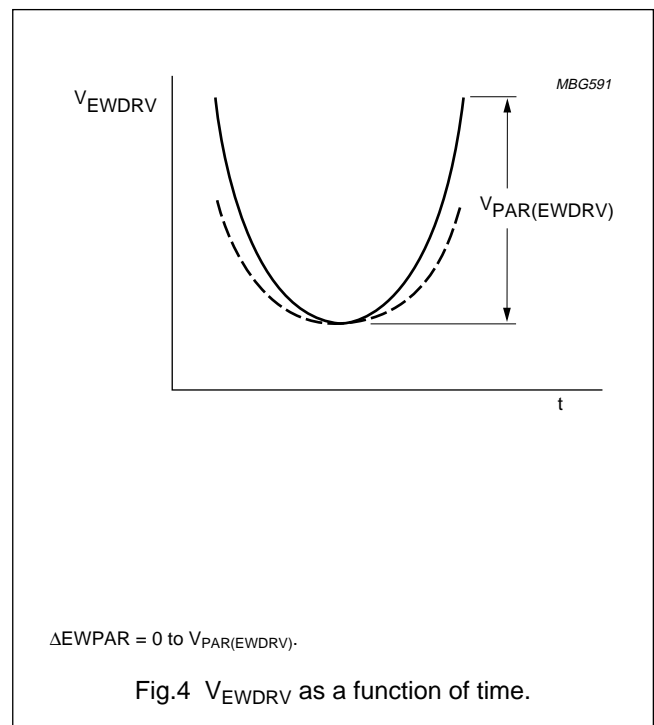
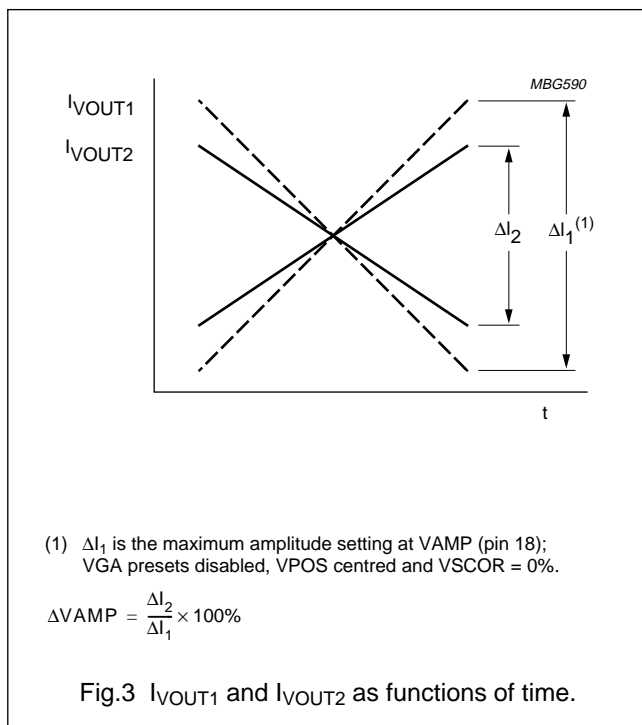
1. For duration of vertical blanking pulse see characteristics of "Vertical oscillator (oscillator frequency in application without adjustment of free-running frequency $f_{V(O)}$)".
2. Continuous blanking at CLBL (pin 16) will be activated, if one of the following conditions is true:
 - a) No horizontal flyback pulses at HFLB (pin 1) within a line
 - b) X-ray protection is triggered
 - c) Voltage at HPLL2 (pin 31) is low (for soft start of horizontal drive)
 - d) Supply voltage at V_{CC} (pin 9) is low
 - e) PLL1 unlocked while frequency-locked loop is in search mode.
3. To ensure safe locking of the horizontal oscillator, one of the following procedures is required:
 - a) Search mode starts always from f_{min} . Then the PLL1 filter components are a 3.3 nF capacitor from pin 26 to ground in parallel with an 8.2 k Ω resistor in series with a 47 nF capacitor.
 - b) Search mode starts either from f_{min} or f_{max} with HPOS in middle position ($I_{HPOS} = 60 \mu A$). Then the PLL1 filter components are a 1.5 nF capacitor from pin 26 to ground in parallel with a 27 k Ω resistor in series with a 47 nF capacitor.
 - c) After locking is achieved, HPOS can be operated in the normal way.
4. Loading of HPLL1 (pin 26) is not allowed.
5. Oscillator frequency is f_{min} when no sync input signal is present (no continuous blanking at pin 16).
6. Voltage at HPLL1 (pin 26) is fed to HBUF (pin 27) via a buffer. Disturbances caused by horizontal sync are removed by an internal sample-and-hold circuit.
7. Input resistance at HPOS (pin 30): $R_{HPOS} = \frac{kT}{q} \times \frac{1}{I_{HPOS}}$
8. Full vertical sync range with constant amplitude ($f_{V(min)} : f_{V(max)} = 1 : 2.5$) can be made usable by choosing an application with adjustment of free-running frequency.
9. If higher vertical frequencies are required, sync range can be shifted by using a smaller capacitor at VCAP (pin 24).
10. Value of resistor at VREF (pin 23) may not be changed.
11. All vertical and EW adjustments are specified at nominal vertical settings, which means:
 - a) $\Delta V_{AMP} = 100\%$ ($I_{VAMP} = 135 \mu A$)
 - b) $\Delta V_{SCOR} = 0$ (pin 19 open-circuit)
 - c) ΔV_{POS} centred (pin 17 forced to ground)
 - d) VGA presets disabled (current ratio $I_{HBUF} : I_{HREF} < 2.25$)
 - e) $f_H = 70$ kHz.
12. VGA presets are enabled below the horizontal frequency at which the current ratio $I_{HBUF} : I_{HREF}$ exceeds the specified value.
13. The superimposed logarithmic sawtooth at VSCOR (pin 19) tracks with internal VGA settings and with VPOS, but **not** with VAMP settings. The superimposed waveform is described by $\frac{kT}{q} \times \ln \frac{1-d}{1+d}$ with 'd' being the modulation depth of a sawtooth from $-\frac{5}{6}$ to $+\frac{5}{6}$. A linear sawtooth with the same modulation depth can be recovered in an external long-tailed pair (see Fig.17).
14. The output signal at EWDRV (pin 11) may consist of parabola + DC shift + trapezium correction. These adjustments have to be carried out in a correct relationship to each other in order to avoid clipping due to the limited output voltage range at EWDRV.

Autosync Deflection Controller (ASDC)

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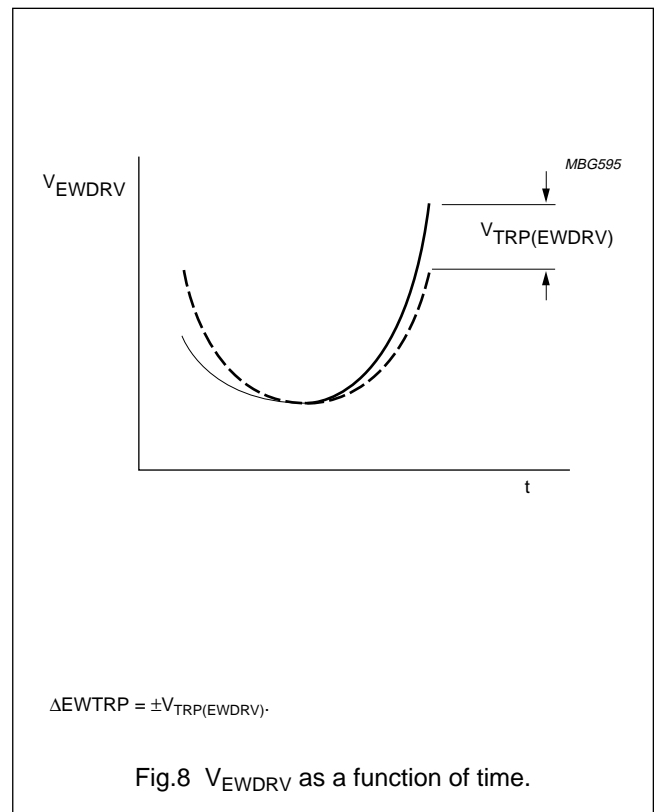
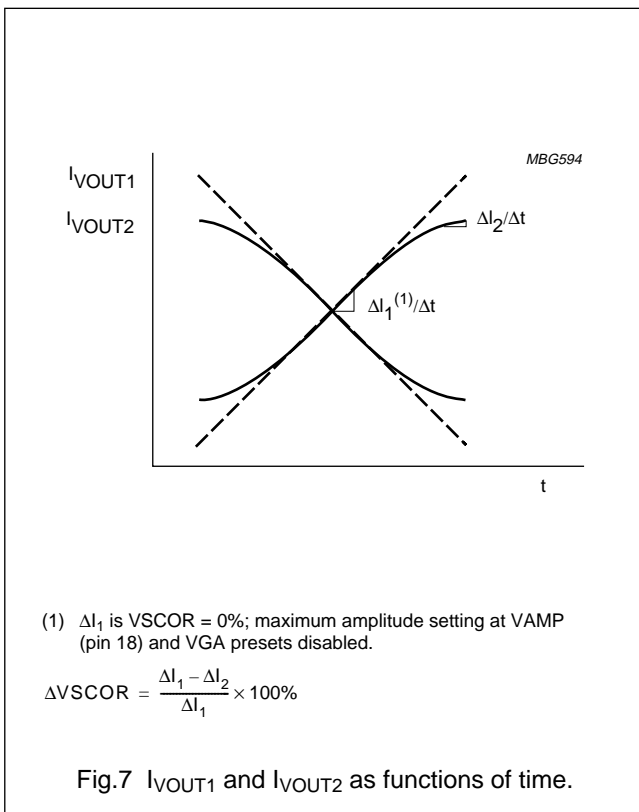
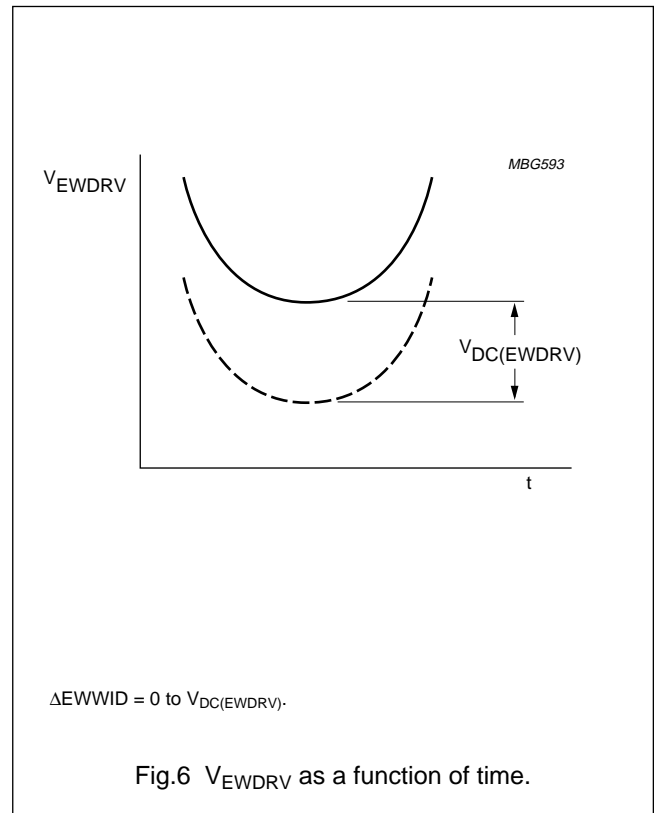
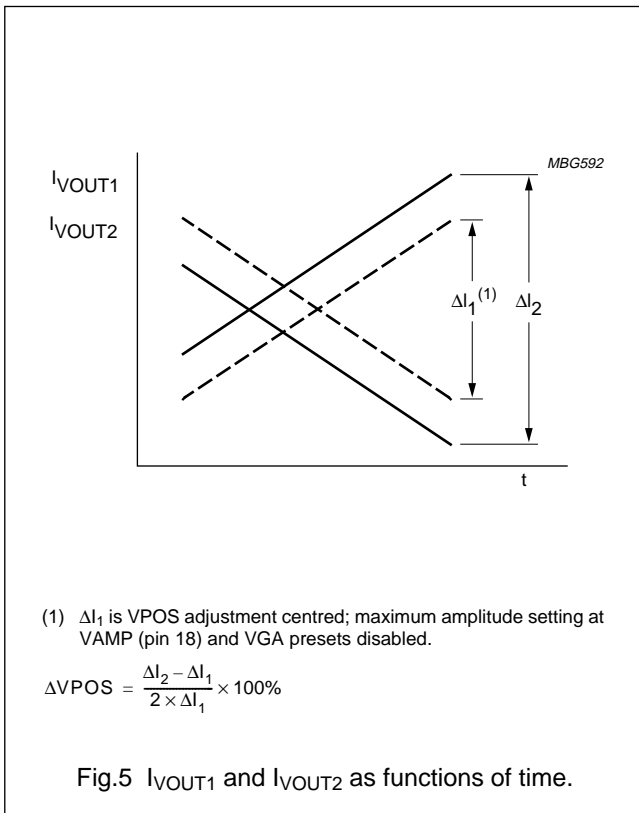
- 15. The superimposed logarithmic parabola at EWTRP (pin 20) tracks with internal VGA settings and with VPOS, but **not** with VAMP settings (see Fig.17).
- 16. If f_H tracking is enabled, the amplitude of the complete EWDRV output signal (parabola + DC shift + trapezium) will be changed proportional to I_{HREF} . The EWDRV low level of 1.2 V remains fixed.
- 17. First pole of transconductance amplifier is 5 MHz without external capacitor (will become the second pole, if the OTA operates as an integrator).
- 18. Open-loop gain is $\frac{V_{BOP}}{V_{BIN}}$ at $f = 0$ with no resistive load and $C_{BOP} = 4.7$ nF (from BOP (pin 3) to GND).

Vertical and EW adjustments



Autosync Deflection Controller (ASDC)

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Autosync Deflection Controller (ASDC)

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Pulse diagrams

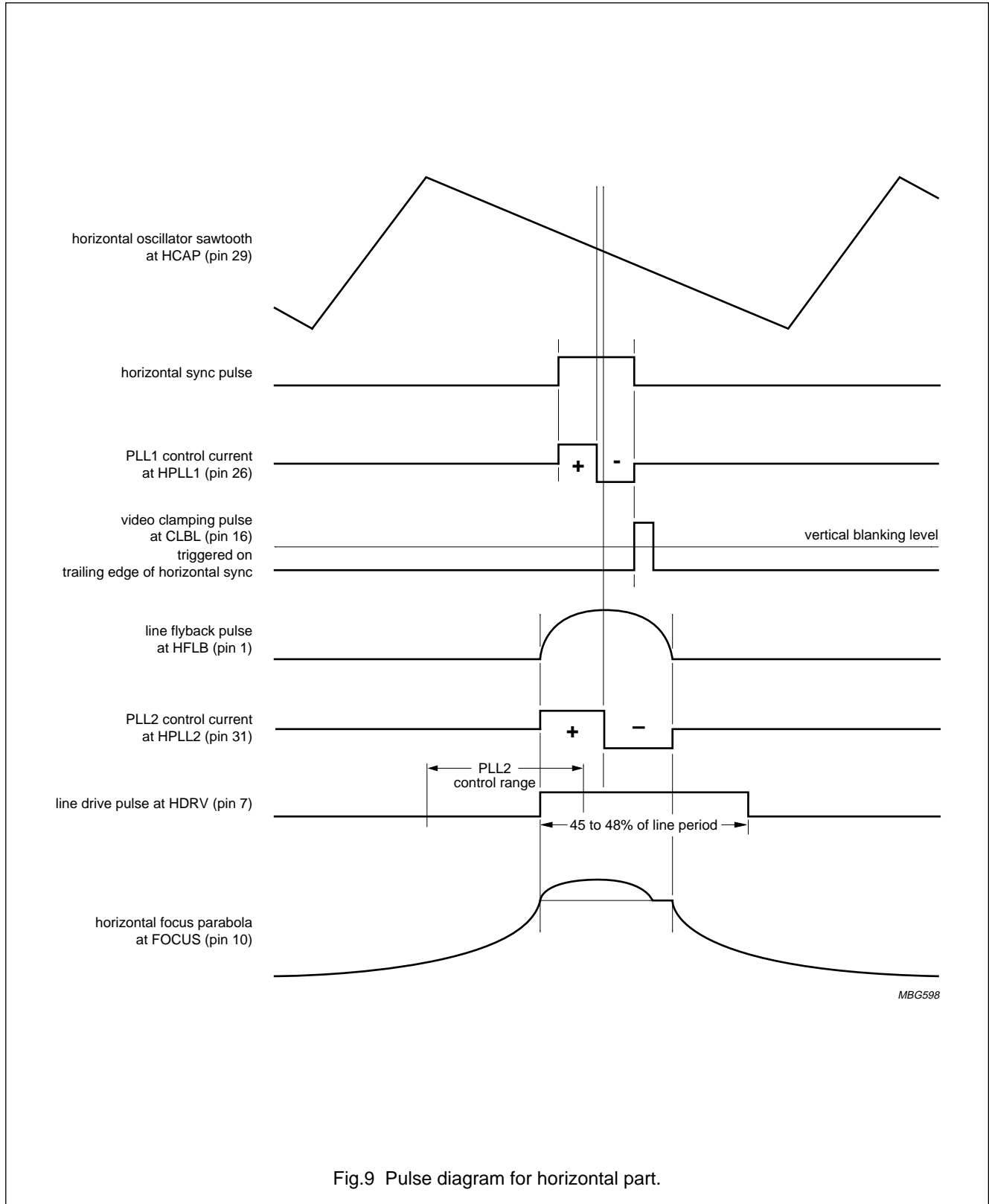


Fig.9 Pulse diagram for horizontal part.

Autosync Deflection Controller (ASDC)

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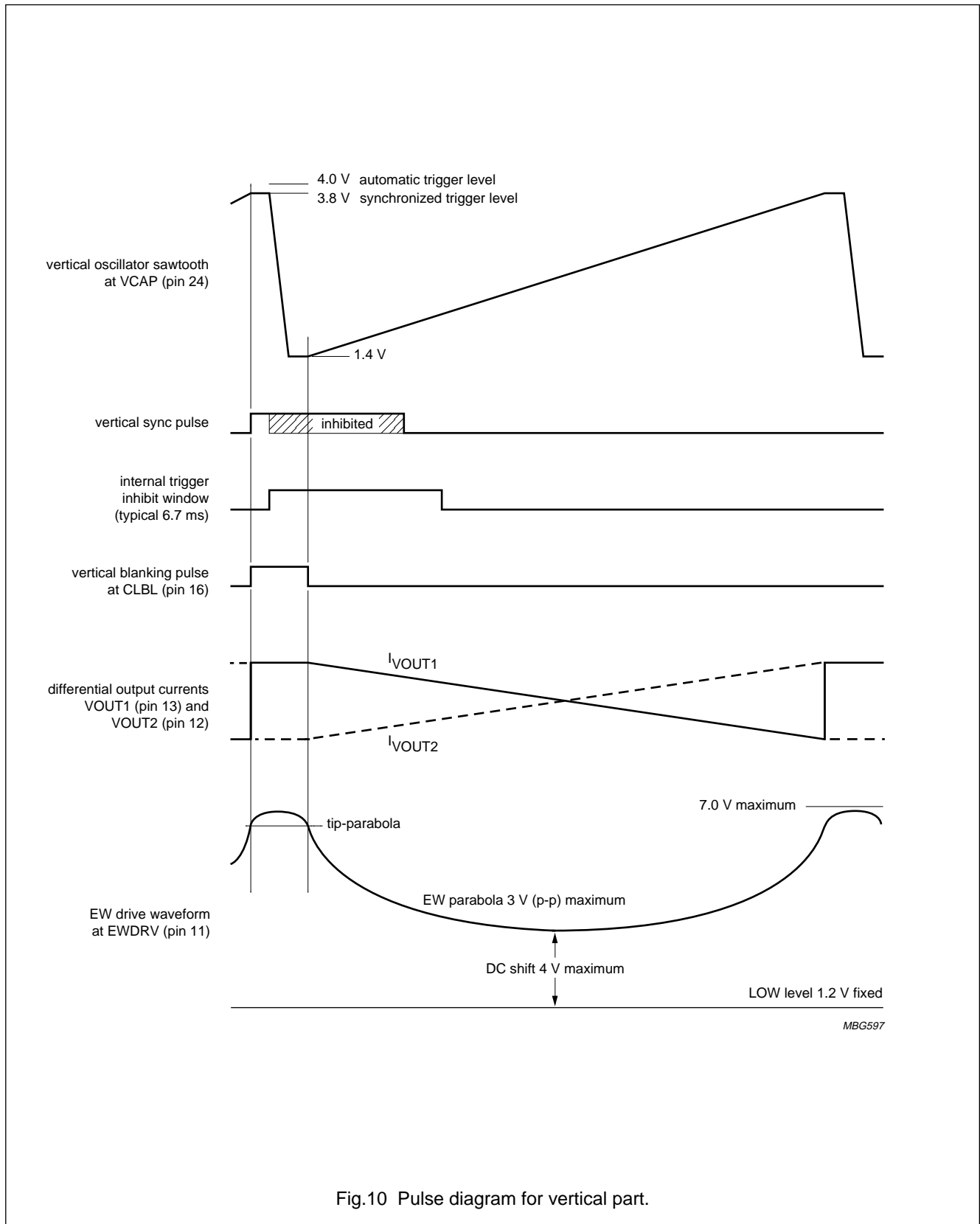
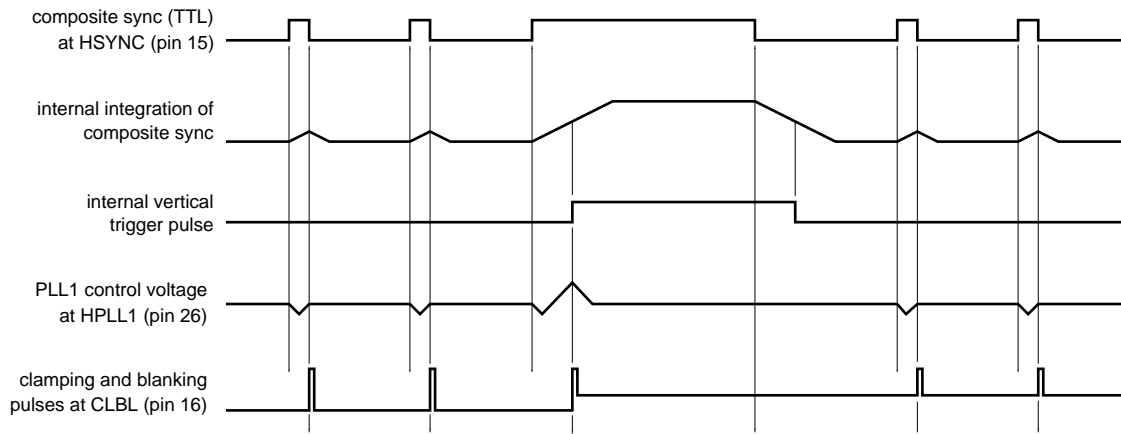


Fig.10 Pulse diagram for vertical part.

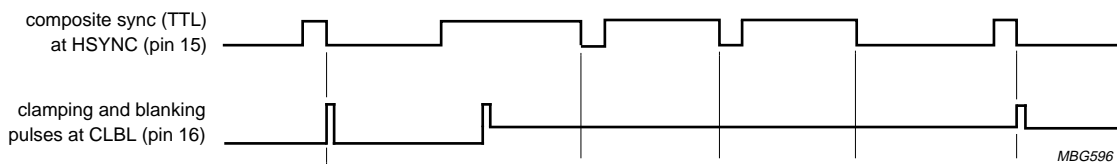
Autosync Deflection Controller (ASDC)

TDA4855



MGC947

a. Reduced influence of vertical sync on horizontal phase.



MBG596

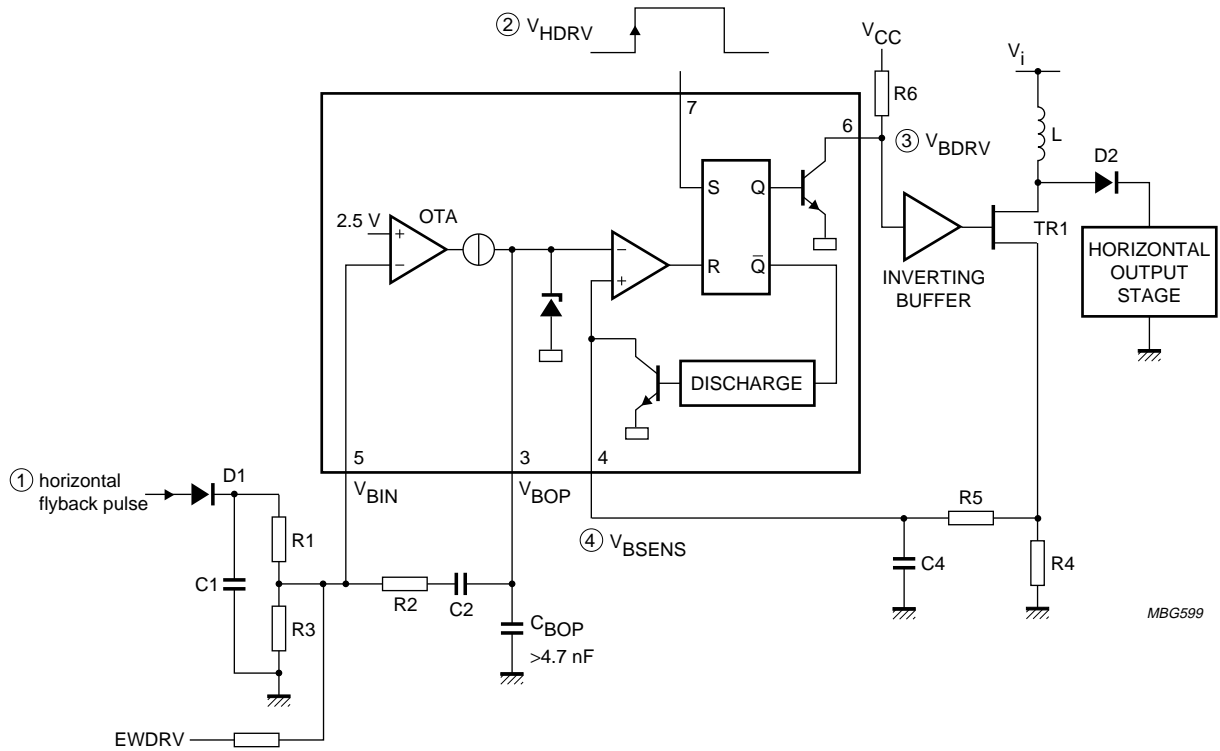
b. Generation of video clamping pulses during vertical sync with serration pulses.

Fig.11 Pulse diagrams for composite sync applications.

Autosync Deflection Controller (ASDC)

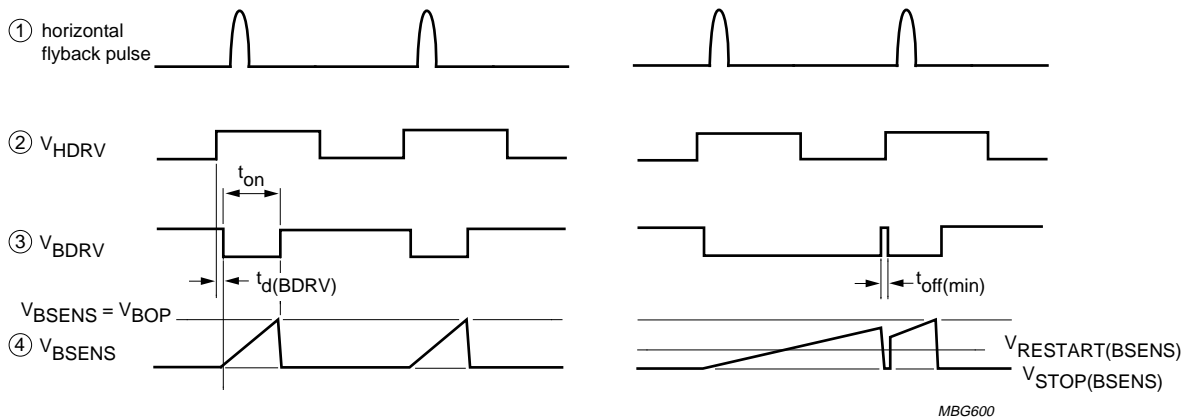
TDA4855

APPLICATION INFORMATION



For $f < 50$ kHz and $C2 < 47$ nF calculation formulas and behaviour of the OTA are the same as for an OP. An exception is the limited output current at BOP (pin 3). See Chapter "Characteristics", Row Head "B+ control section (see Figs 12 and 13)".

a. Feedback mode application.



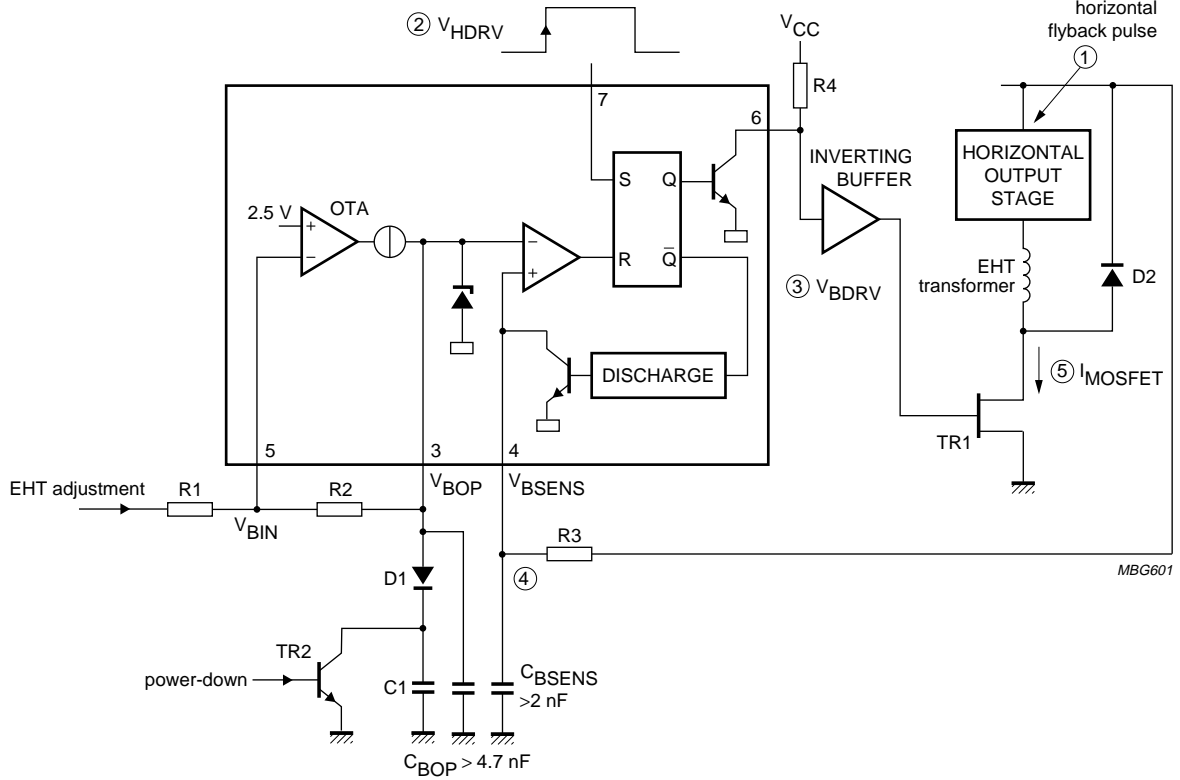
b. Waveforms for normal operation.

c. Waveforms for fault condition.

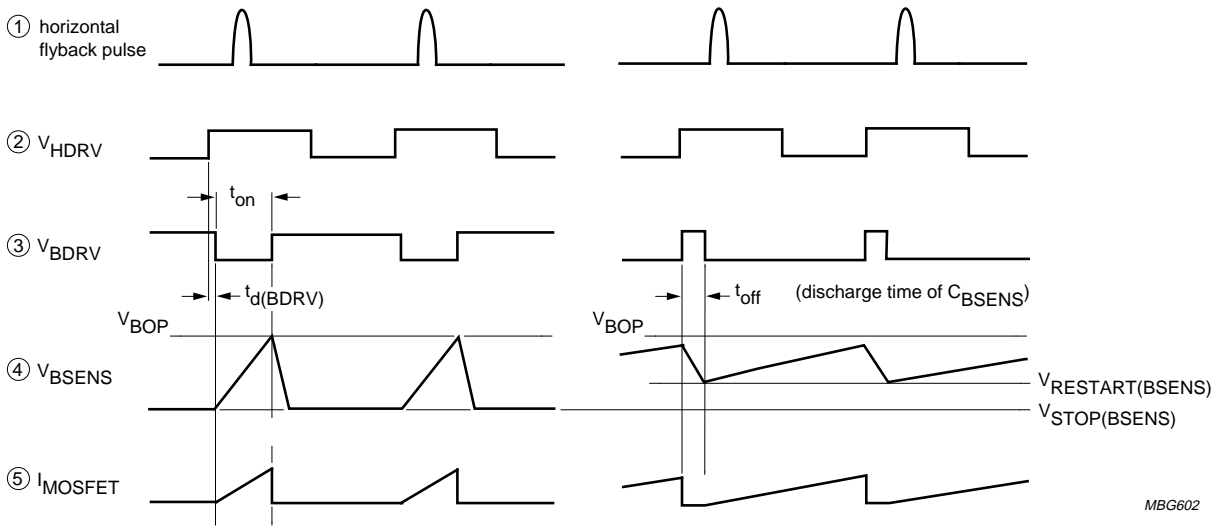
Fig.12 Application and timing for feedback mode.

Autosync Deflection Controller (ASDC)

TDA4855



a. Forward mode application.



b. Waveforms for normal operation.

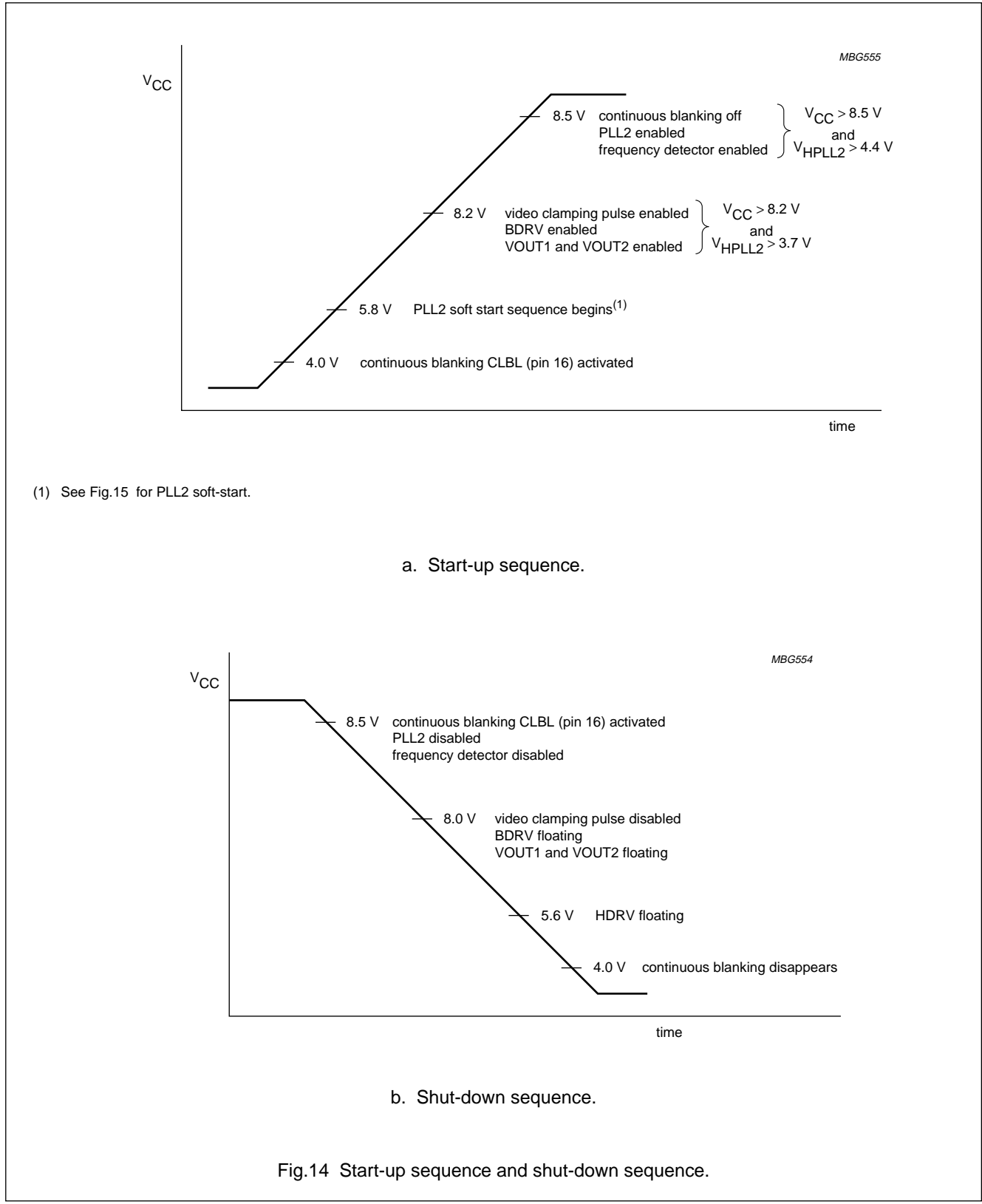
c. Waveforms for fault condition.

Fig.13 Application and timing for feed forward mode.

Autosync Deflection Controller (ASDC)

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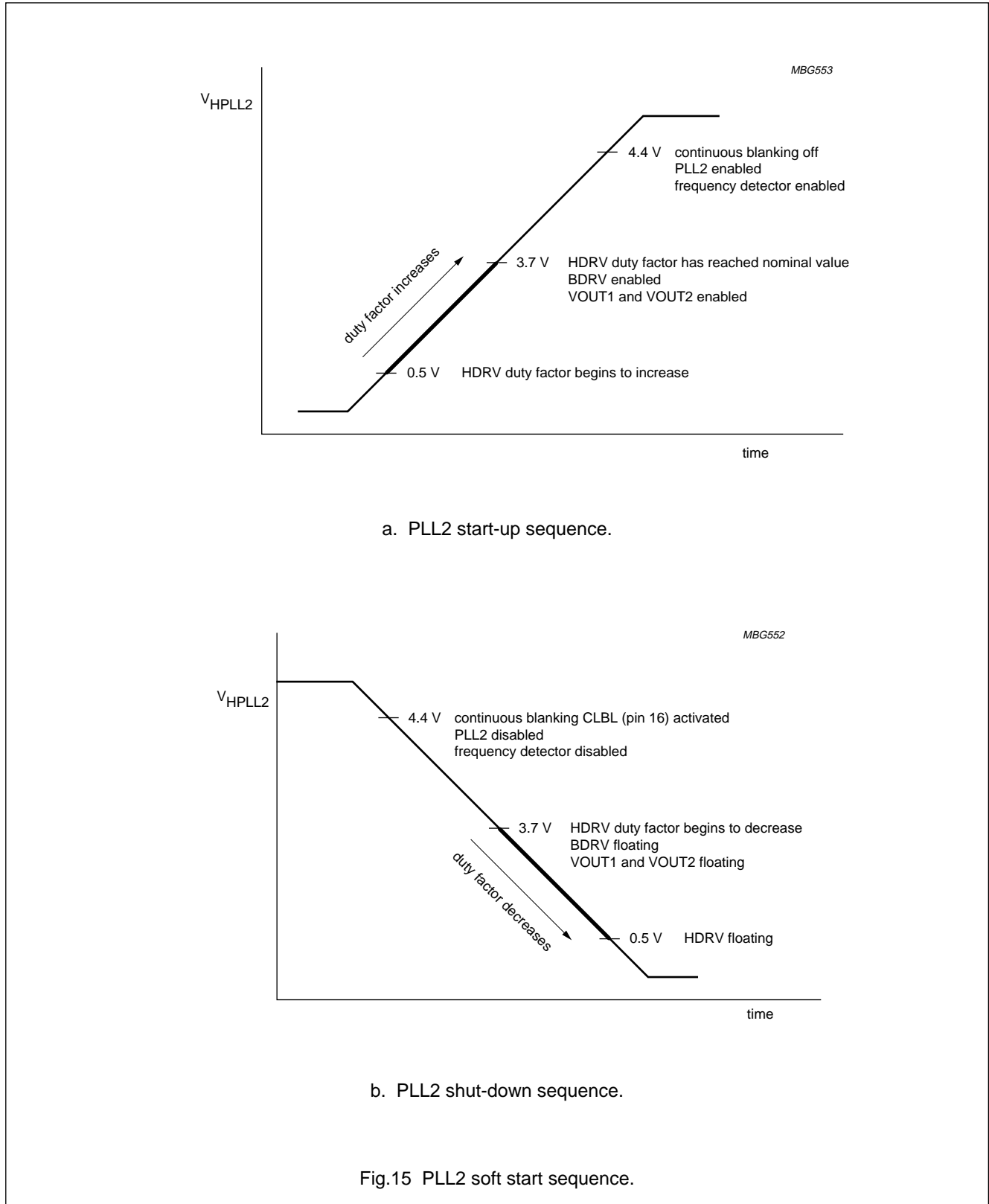
Start-up and shut-down sequence



Autosync Deflection Controller (ASDC)

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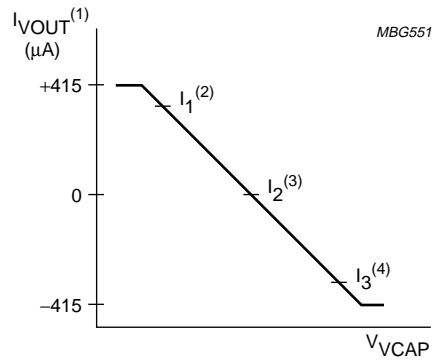
PLL2 soft start sequence



Autosync Deflection Controller (ASDC)

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Vertical linearity error



- (1) $I_{VOUT} = I_{VOUT1} - I_{VOUT2}$.
 (2) $I_1 = I_{VOUT}$ at $V_{VCAP} = 1.9$ V.
 (3) $I_2 = I_{VOUT}$ at $V_{VCAP} = 2.6$ V.
 (4) $I_3 = I_{VOUT}$ at $V_{VCAP} = 3.3$ V.

Which means: $I_0 = \frac{I_1 - I_3}{2}$

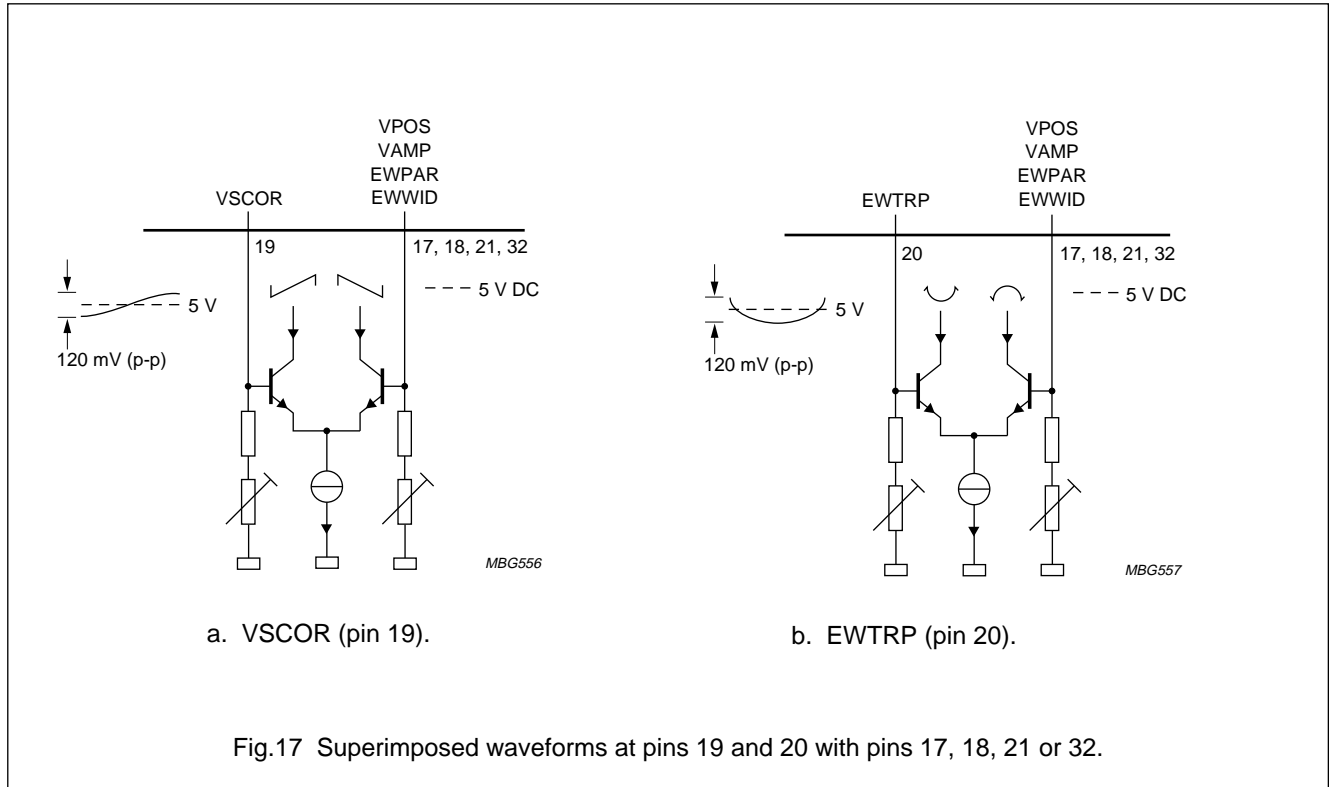
Vertical linearity error = $1 - \max\left(\frac{I_1 - I_2}{I_0} \text{ or } \frac{I_2 - I_3}{I_0}\right)$

Fig.16 Definition of vertical linearity error.

Autosync Deflection Controller (ASDC)

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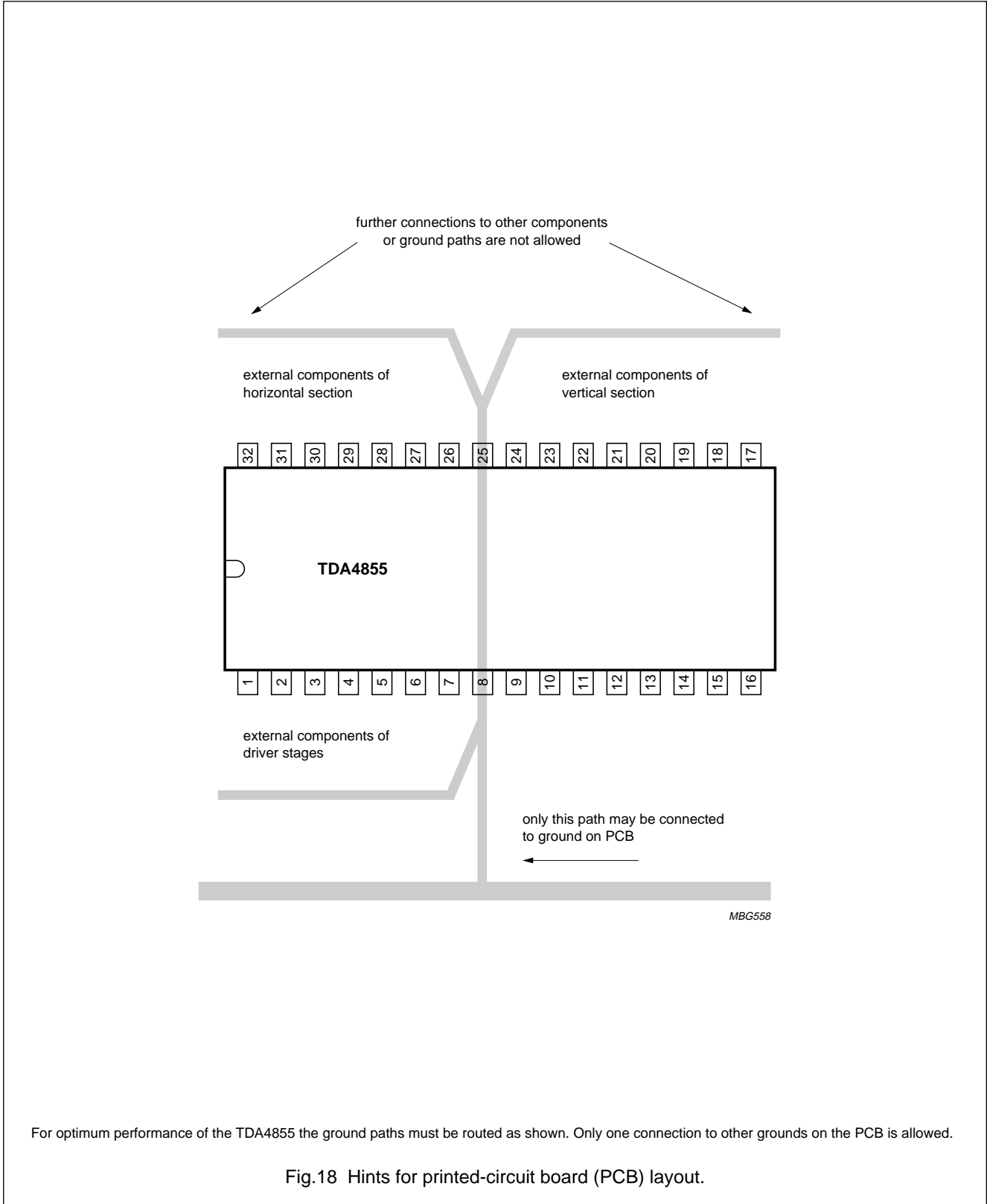
Usage of superimposed waveforms



Autosync Deflection Controller (ASDC)

TDA4855

Printed printed-circuit board layout



For optimum performance of the TDA4855 the ground paths must be routed as shown. Only one connection to other grounds on the PCB is allowed.

Fig.18 Hints for printed-circuit board (PCB) layout.

Autosync Deflection Controller (ASDC)

TDA4855

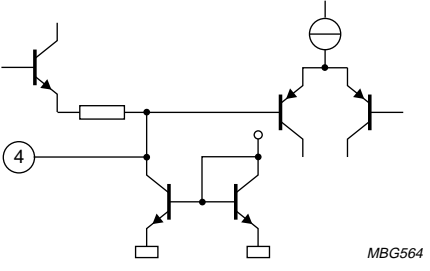
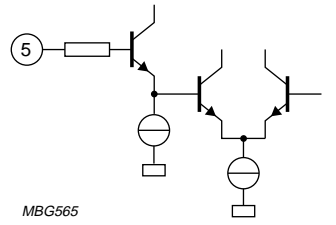
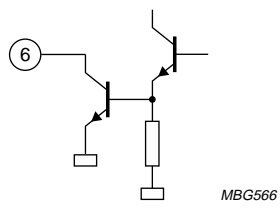
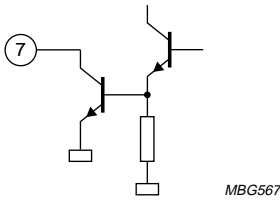
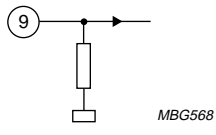
INTERNAL CIRCUITRY

Table 5 Internal circuitry of Fig.1

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|------------------|
| 1 | HFLB | |
| 2 | XRAY | |
| 3 | BOP | |

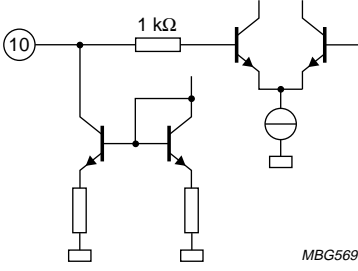
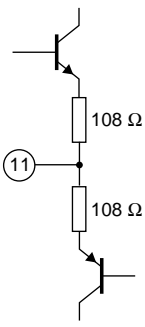
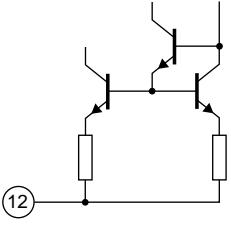
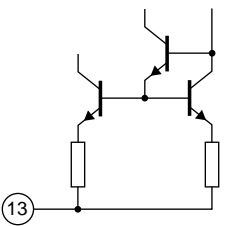
Autosync Deflection Controller (ASDC)

TDA4855

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|-----------------|--|
| 4 | BSENS |  <p style="text-align: right;"><i>MBG564</i></p> |
| 5 | BIN |  <p style="text-align: right;"><i>MBG565</i></p> |
| 6 | BDRV |  <p style="text-align: right;"><i>MBG566</i></p> |
| 7 | HDRV |  <p style="text-align: right;"><i>MBG567</i></p> |
| 8 | PGND | power ground, connected to substrate |
| 9 | V _{CC} |  <p style="text-align: right;"><i>MBG568</i></p> |

Autosync Deflection Controller (ASDC)

TDA4855

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|---|
| 10 | FOCUS |  <p style="text-align: right;">MBG569</p> |
| 11 | EWDRV |  <p style="text-align: right;">MBG570</p> |
| 12 | VOUT2 |  <p style="text-align: right;">MBG571</p> |
| 13 | VOUT1 |  <p style="text-align: right;">MBG572</p> |

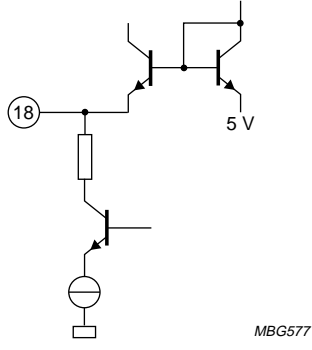
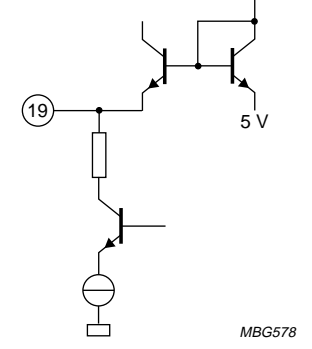
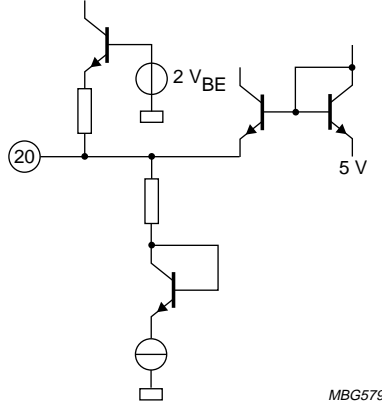
Autosync Deflection Controller (ASDC)

TDA4855

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|---|
| 14 | VSYNC | <p style="text-align: right;"><i>MBG573</i></p> |
| 15 | HSYNC | <p style="text-align: right;"><i>MBG574</i></p> |
| 16 | CLBL | <p style="text-align: right;"><i>MBG575</i></p> |
| 17 | VPOS | <p style="text-align: right;"><i>MBG576</i></p> |

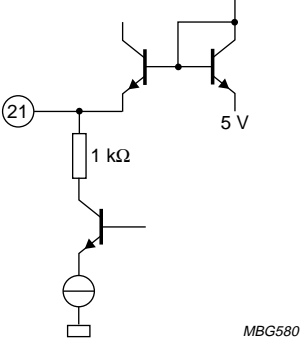
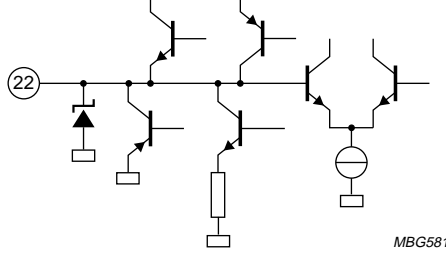
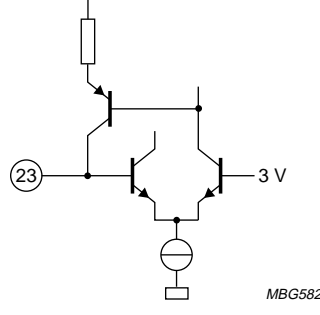
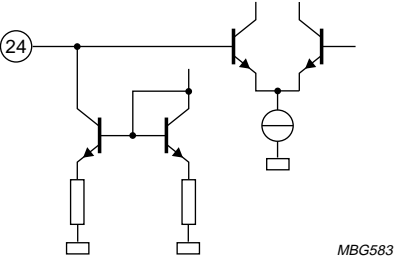
Autosync Deflection Controller (ASDC)

TDA4855

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|---|
| 18 | VAMP |  <p style="text-align: right;">MBG577</p> |
| 19 | VSCOR |  <p style="text-align: right;">MBG578</p> |
| 20 | EWTRP |  <p style="text-align: right;">MBG579</p> |

Autosync Deflection Controller (ASDC)

TDA4855

| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|--|
| 21 | EWPAR |  |
| 22 | VAGC |  |
| 23 | VREF |  |
| 24 | VCAP |  |
| 25 | SGND | signal ground |

Autosync Deflection Controller (ASDC)

TDA4855

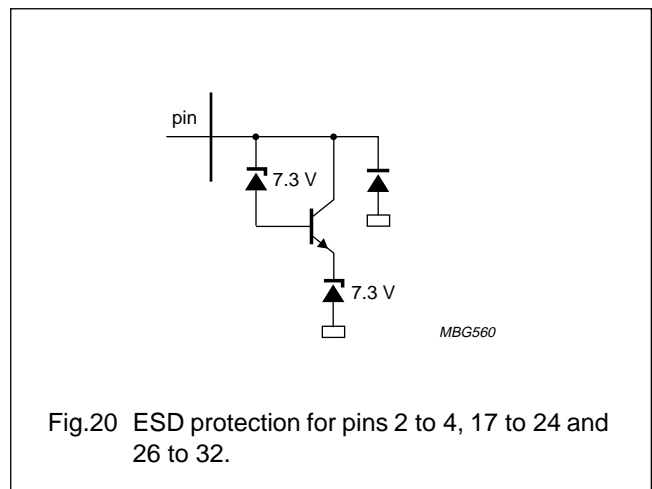
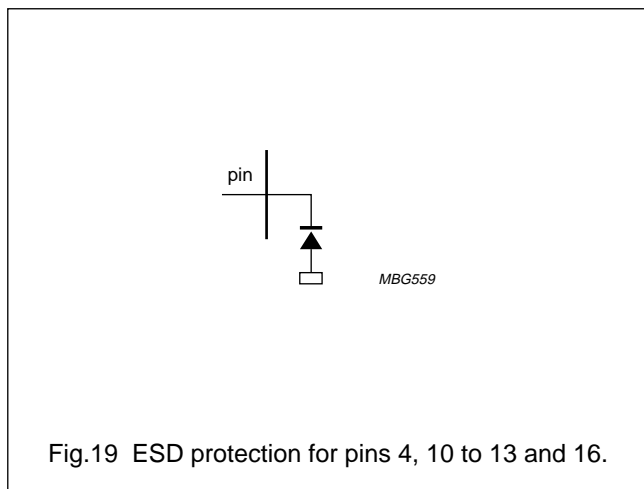
| PIN | SYMBOL | INTERNAL CIRCUIT |
|----------|--------------|------------------|
| 26 | HPLL1 | |
| 27 | HBUF | |
| 28 29 | HREF HCAP | |
| 30 | HPOS | |

Autosync Deflection Controller (ASDC)

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| PIN | SYMBOL | INTERNAL CIRCUIT |
|-----|--------|------------------|
| 31 | HPLL2 | |
| 32 | EWWID | |

Electrostatic discharge (ESD) protection



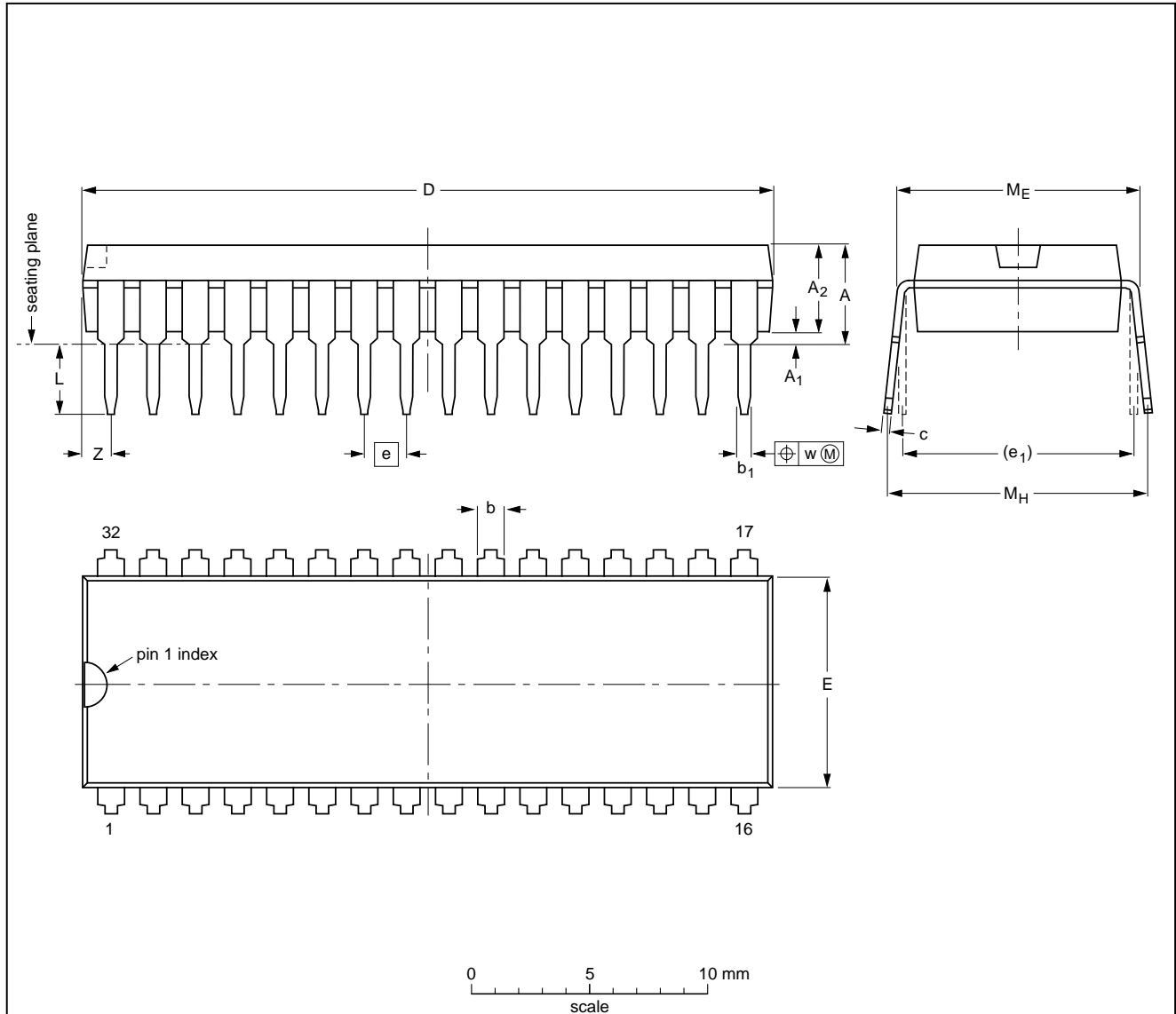
Autosync Deflection Controller (ASDC)

TDA4855

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)

SOT232-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|------|--------|---------------------|---------------------|------------|----------------|--------------|------------------|------------------|-------|----------------|------------|----------------|----------------|------|-----------------------|
| mm | 4.7 | 0.51 | 3.8 | 1.3 0.8 | 0.53 0.40 | 0.32 0.23 | 29.4 28.5 | 9.1 8.7 | 1.778 | 10.16 | 3.2 2.8 | 10.7 10.2 | 12.2 10.5 | 0.18 | 1.6 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT232-1 | | | | | | 92-11-17 95-02-04 |

Autosync Deflection Controller (ASDC)

TDA4855

SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

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Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 83749, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
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Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
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252148 KIEV, Tel. +380 44 476 0297/1642, Fax. +380 44 476 6991

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 825 344, Fax. +381 11 635 777

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